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The Roadrunner Trap

A QSCOUT Device

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The Roadrunner Trap

Microfabricated Surface Electrode Junction Ion Trap

ABSTRACT

The Roadrunner ion trap is a micro-fabricated surface-electrode ion trap based on silicon technology. This trap has one long linear section and a junction to allow for chain storage and reconfiguration. It uses a symmetric rf-rail design with segmented inner and outer control electrodes and independent control in the junction arms. The trap is fabricated on Sandia's High Optical Access (HOA) platform to provide good optical access for tightly focused laser beams skimming the trap surface. It is packaged on our custom Bowtie-102 ceramic pin or land grid array packages using a 2.54 mm pitch for backside pins or pads. This trap also includes an rf sensing capacitive divider and tungsten wires for heating or temperature monitoring. The Roadrunner builds on the knowledge gained from previous surface traps fabricated at Sandia [1, 2, 3] while improving ion control capabilities.

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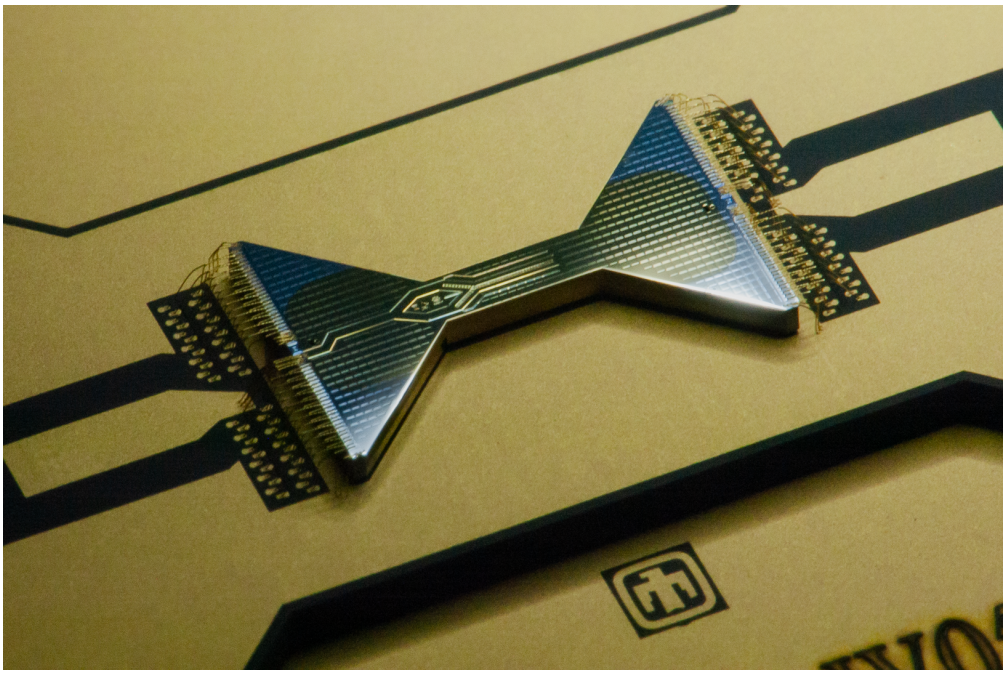

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1. INTRODUCTION

The Roadrunner trap is a single-junctioned surface trap in a 'Y' shape that was developed at Sandia National Laboratories for the Quantum Scientific Computing Open User Testbed (QSCOUT) project funded by the Department of Energy, Office of Science, ASCR Testbed program [4] (see Fig. 1-1). The purpose of this device is to hold a chain of ions in a single potential well in the center of the long linear region (called the 'quantum' region), with each ion addressed by a tightly focused laser beam. The junction and 'legs' of this device are intended for storing and reordering of ions while a subset of ions are measured in the quantum region. This measurement of a subset of ions while some are protected is known as a mid-circuit measurement, and can reduce requirements on ion number and circuit depths for quantum computing circuits [5].

Trap properties that are important to realize the dual goals of high-fidelity quantum gates and the ability to store and reorder ions for mid-circuit measurements include:

- High optical access for tightly focused laser beams skimming the surface of the trap perpendicular to the trap axis.
- A loading region separate from the region used for quantum operations.
- High radio-frequency (rf) voltage efficiency (low loss into the device) and sufficiently large radial trap frequencies to enable high-fidelity quantum gates.
- Minimization of rf dissipation on the device to facilitate consistent trap operation and to reduce the heat load for operation at cryogenic temperatures.
- Chip-scale capacitors to ensure that dc control electrodes are shielded from the strong rf.
- Full and independent control of all degrees of freedom of the trapping potential.
- Good axial voltage efficiency (able to achieve tight frequencies with a low voltage budget $< 10\,\mathrm{V}$) to enable precise control of axial trapping fields as well as to realize separation and merging of ion chains.
- Constant pseudo-potential magnitude (except near junctions) throughout the entire trap to enable ion shuttling though the device while maintaining constant trapping conditions.

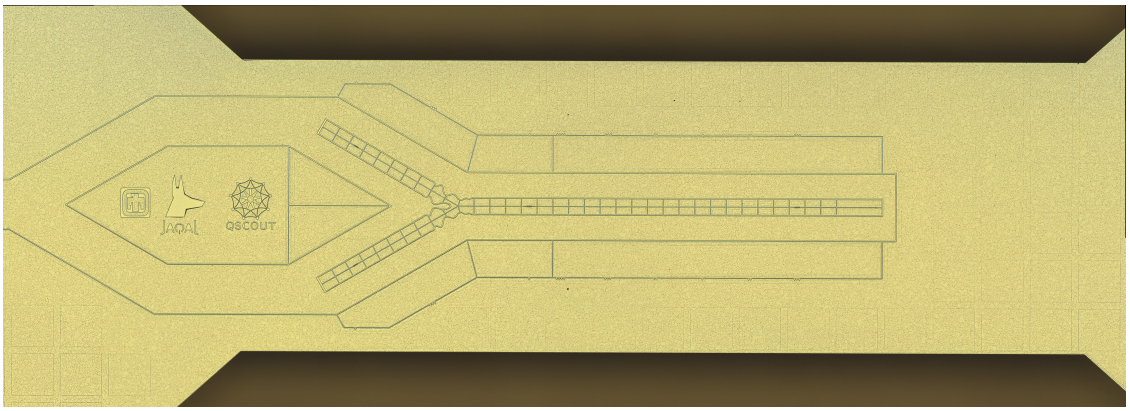

Figure 1-1.: Optical image of the trapping region and rf split in the Roadrunner trap. The junction is within the isthmus of the trap allowing for laser access where the numerical aperture is highest to minimize potential clipping.

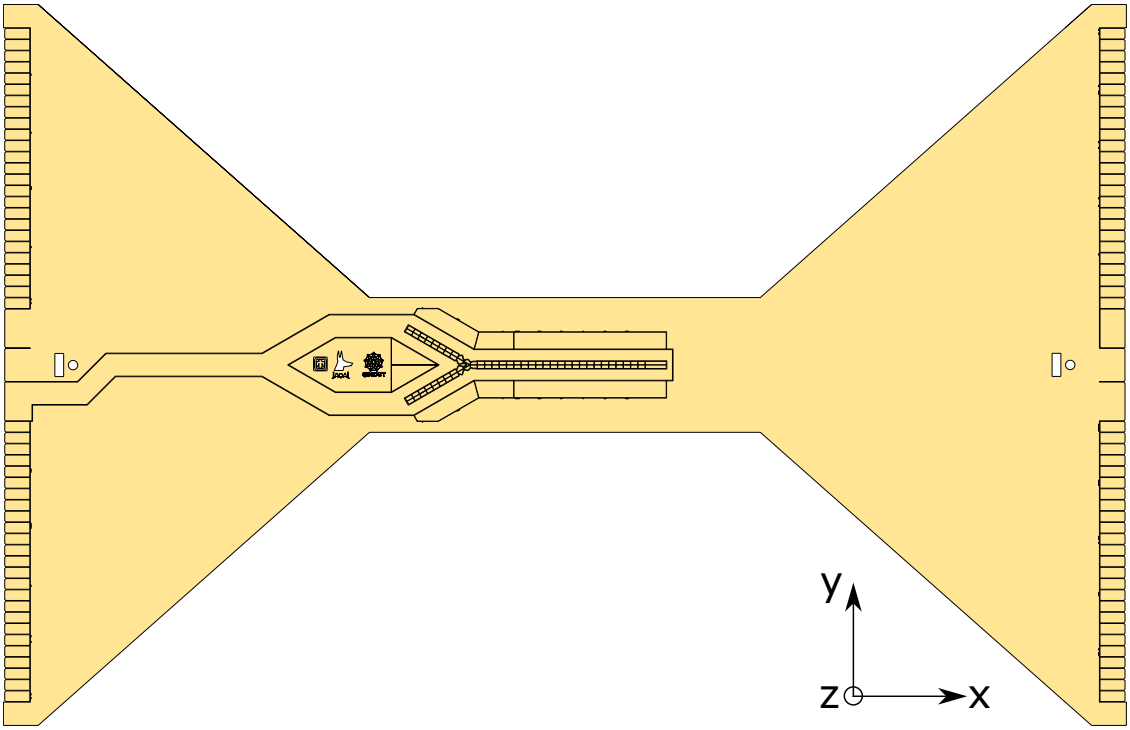

Figure 1-2.: Schematic of the Roadrunner Trap showing the electrode position on the HOA platform. Both the junction and the quantum region are within the isthmus allowing for each to be addressed without clipping lasers on the trap or package. The platform has a bowtie shape where the wide 'wings' accommodate wirebonding to the 100 signal connections, including 2 rf connections that are used for rf feed and rf probe (see Sec. 4.2), as well as an aluminum wire for temperature sensing and a tungston wire for heating (see Sec. 4.3). Additional ground wirebonds can be attached at two dedicated bondpads as well as the four corners of the substrate.

2. TOP METAL TRAP DESIGN

2.1. Trap Geometry

The top metal of the Roadrunner trap consists of a long linear section with a junction and two shorter legs (see Figs. 1-2 and 2-1). The shapes of the inner dc electrodes and the rf rails in the transition regions between the junction and the linear sections are modulated to reduce axial rf pseudopotential barriers and to enable shuttling through the transition while keeping all trap frequencies and principal axes constant (see Sec. 2.4).

We define the coordinate system with the x-axis in the plane of the top metal level along the long linear region of the trap, the y-axis in the plane of the trap surface perpendicular to the linear axis of the trap, and the z-axis perpendicular to the trap surface (see Figure 1-2). The origin of the coordinate system is at the center of linear region of the trap (the L electrodes), between electrodes L25, L26, L27, and L28 in Fig. 2-1. In the vertical direction $z = 0$ is defined as the top of the top metal level and thus the ion trapping location is at about $z = +0.068$ mm.

2.2. Rf Pseudo-Potential

To optimize the electrode configurations such as rf electrode widths, gaps, and inner control electrode size, we looked at a variety of factors which included: ion height, trap depth, and radial secular frequency. Trap depth is defined by starting at the rf potential node and comparing it to the maximum value as you move away from the trap ($+z$). How rf rail width and separation vary the trap depth, secular frequencies, and ion height is shown in Fig. 2-2. Due to calculations of laser beam scatter off the surface of the trap with ion height, we wanted to maintain a minimum ion height of 65 μm in the quantum region. Additionally, the rf rail is limited to about 100 μm in width to limit capacitance and to fit the junction on the isthmus.

Constraining the ion height to greater than 65 μm, the electrode widths were optimized to jointly give a high trap depth and high trap frequency. Since there is a tradeoff with trap depth and frequency, we chose the values of inner electrode width of 36.5 μm (i.e. rf rail separation of 73 μm) and an rf rail width of 100 μm. From Fig. 2-2, one can see that the compromise point only results in a 10% loss of the trap depth or frequency for a given rf voltage. Additionally, the trap depth and the radial frequencies are dependent on the rf frequency combined with the voltage, not one alone. Using these design parameters, Fig. 2-3 shows the simulated trap depth and radial frequencies for 3 different voltages as a function of rf drive frequency assuming Yb. However, this figure does not show the stability parameter or highlight regions of instability, not all of those lead to a trappable volume.

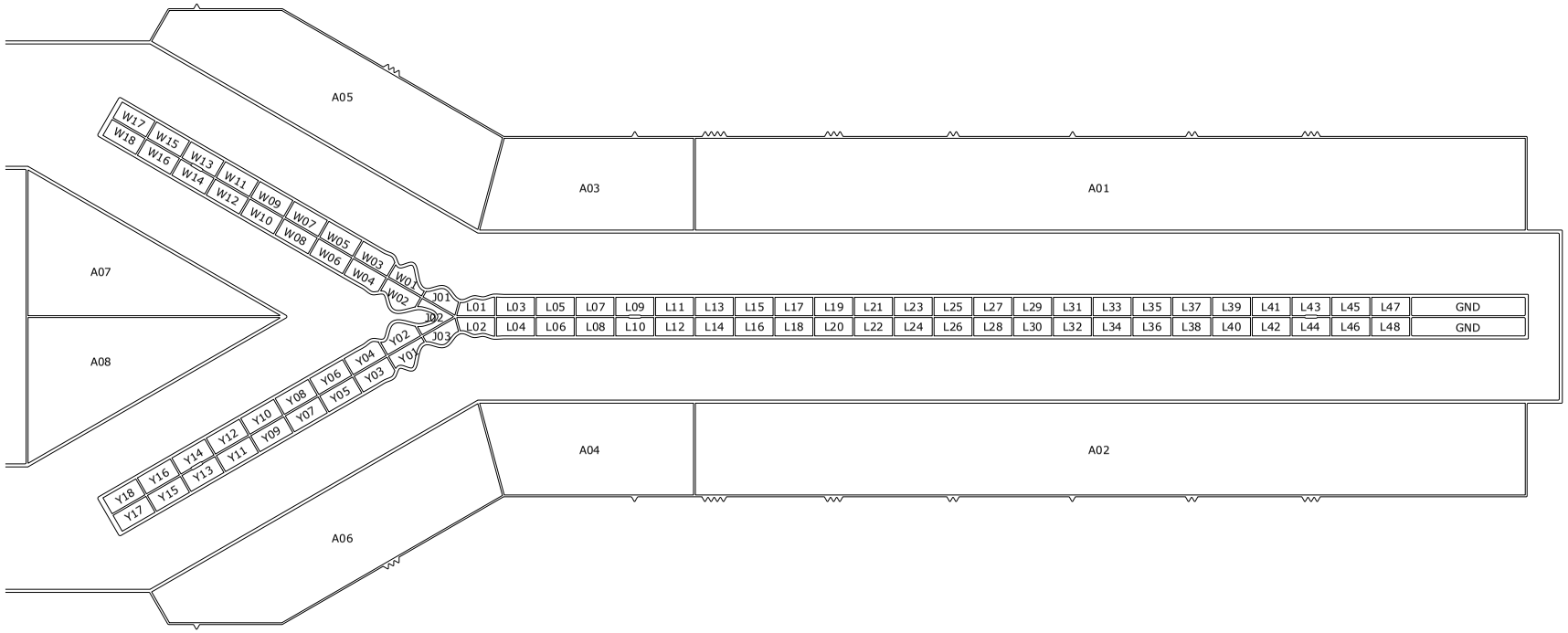

Figure 2-1.: Schematic of the Roadrunner with electrode name labelling There are several different types of dc electrodes on this device. The 'L' electrodes designate electrodes in the 'linear' region, the 'J' electrodes correspond to the 'junction' region. The 'W' and 'Y' electrodes are the upper and lower legs respectively, and the 'A' electrodes are the outer electrodes used primarily for compensation and principal axis rotation. Additionally, there are 4 loading holes distributed across the device. They are centered on electrodes L09/L10, L43/44, Y13/Y14, and W13/W14.

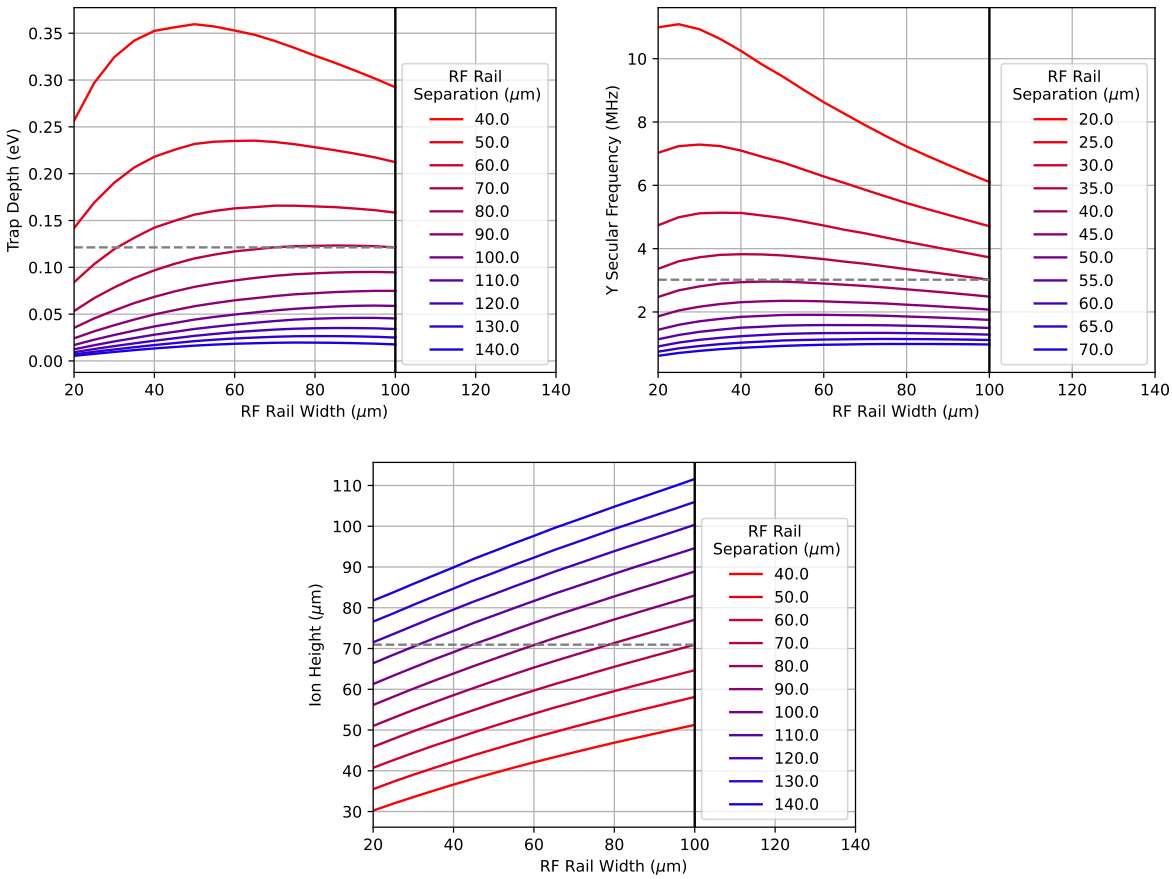

Figure 2-2.: (Top Left) Trap depth, (Top Right) radial frequencies, and (Bottom) ion height versus the rf rail separation for different rail widths. In these figures, the calculated rf drive frequency is 40 MHz, the voltage is 200 V, and the ion is ytterbium. These show that closer, smaller rf rails generally result in a lower ion height and a deeper trap. We chose an ion height of 68 µm, an rf rail width of 100 µm, and a rail separation of 73 µm. The design choices are indicated by the vertical black line and the gray dashed line indicates the corresponding value on the x-axis. This allows us to see, for example, that increasing the rail separation from 70 to 80 would allow us to use a lower rf rail width for the same ion height, but the overall depth is still lower.

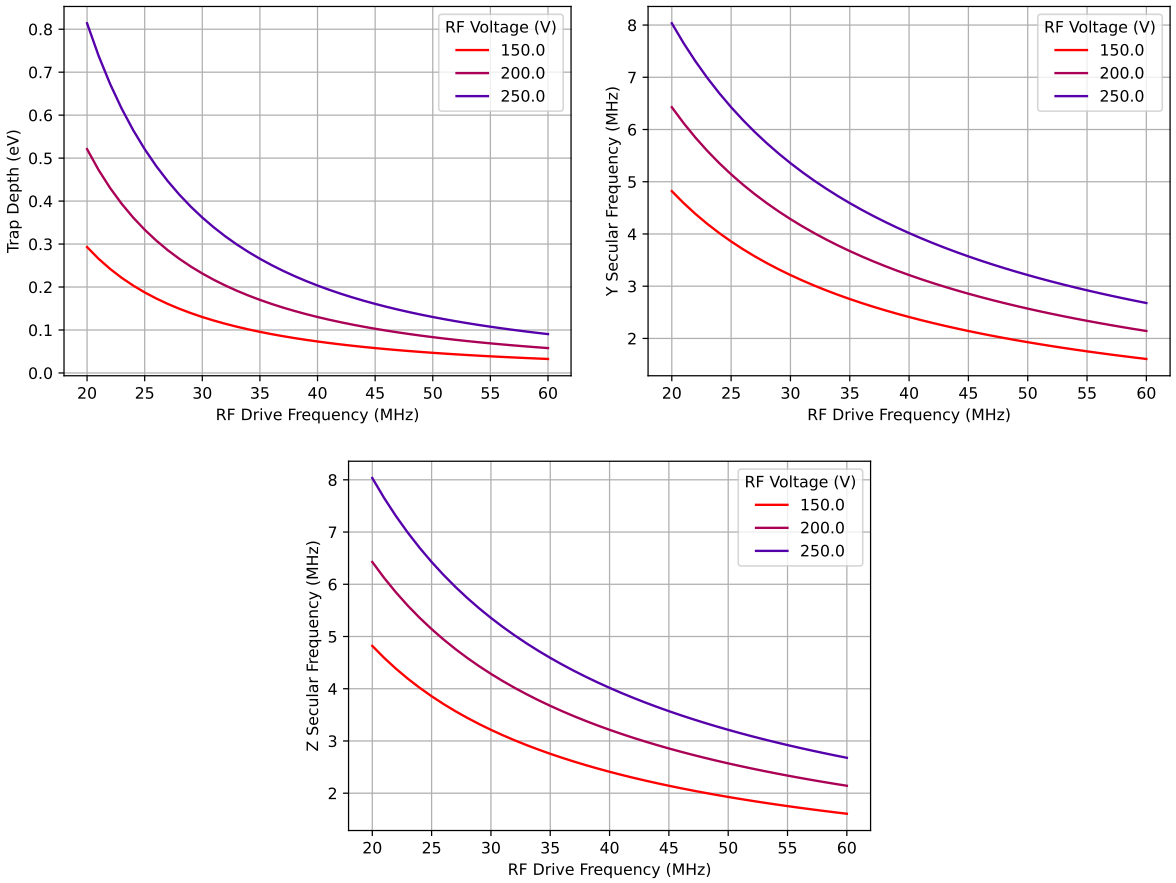

Figure 2-3.: (Top Left) Trap depth, (Top Right) secular y frequency, and (Bottom) secular z frequency versus the rf drive frequency for a Yb ion with 3 different typical voltages given the design choices from Fig. 2-2. Lower drive frequencies result in higher trap depths and radial frequencies, but the drive frequency should be $6-10\times$ larger than the intended radial frequencies.

2.3. Linear Region

The 1.5 mm long central linear region comprises of 24 inner control electrode pairs with a pitch (length) of 65 µm (see Fig. 2-1), where each electrode is completely independent. The residual axial pseudopotential is simulated to be below 5 µeV at the trap center. Because the linear region is partially shared with the junction, the outer electrodes are segmented into 2 pairs, one set surrounding L13-L48 (the quantum region) and a second set around L01-L12 (near the junction). This segmentation allows for ions to pass though the junction with minimal impact on the voltages seen by the chain of ions in the quantum region. In the y-axis (width), the outer electrodes are 150 µm, the rf is 100 µm, and the inner electrodes are 30 µm. This device has no slots, but there are several small holes for backside loading. There are two loading holes in the linear region, centered on L09/L10 and L43/L44.

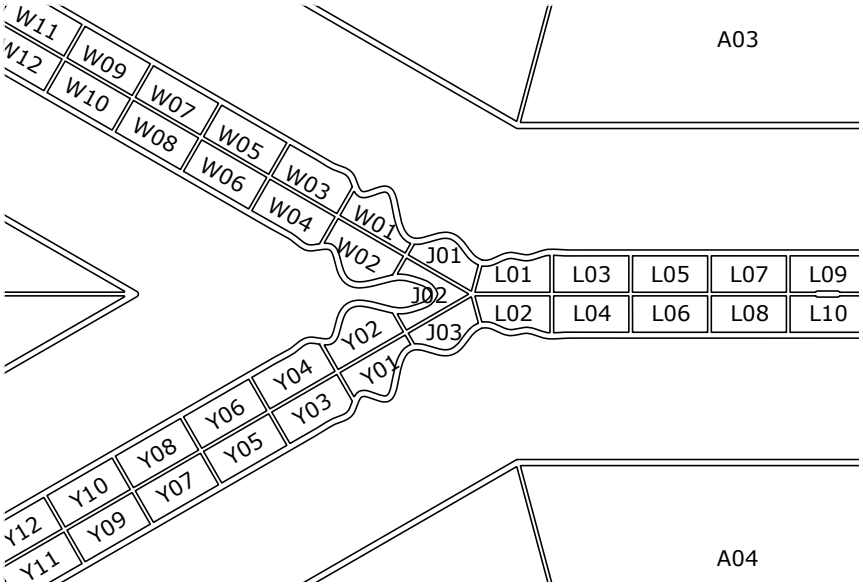

Figure 2-4.: Schematic of the junction region in the Roadrunner Trap. Each leg of the junction is fully independent allowing for the ion(s) to be guided into either leg.

2.4. Junction Region & Optimization

Since the Roadrunner contains a junction, the dc and rf electrode shapes needed to be optimized in order to provide a smooth rf environment to minimize ion heating as the ion is transported through it, a zoomed in schematic is shown in Fig. 2-4. This optimization is done using a nonlinear optimization routine that changes the junction's geometry in order to minimize a cost function. This cost function primarily attempts to minimize the change in several parameters through the junction. These parameters include the ion height (distance of the ion to the surface of the trap), radial frequencies, trap depth, pseudopotential (the effective radial confinement created by the rf voltage when averaged over time), and axial pseudofield (the amount of potential that the rf contributes to the axial direction of the trap - typically small). Fig. 2-5 shows the ion height, secular frequency,

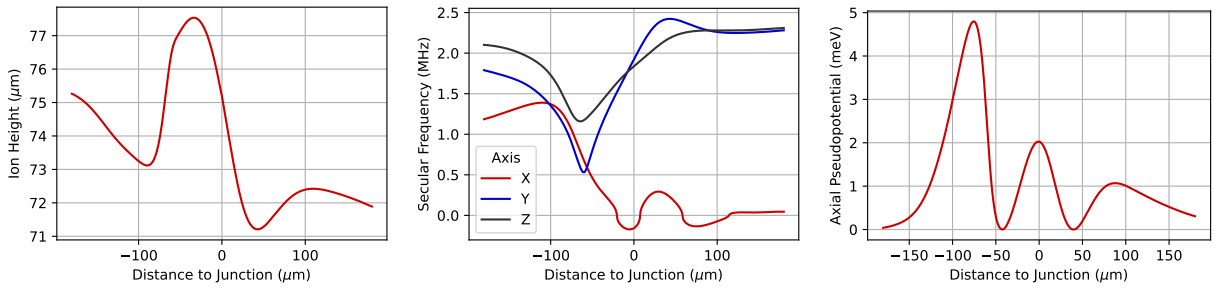

Figure 2-5.: (Left) Ion height, (Center) secular frequencies, and (right) axial pseudopotential through the junction. Negative is further into the junction leg, closer to the RF, and positive to towards the central linear region of the trap. The variation in the axial pseudopotential is leading to the contribution of an axial frequency in and left to the junction. The coordinates at the junction change such that x is always along the trapping access for these plots.

and residual pseudopotential of the ion at positions relative to the junction after optimization. During optimization, the best solution was found when the path of the ion through the junction was allowed to stray off the geometric center of the trap. Once the optimizer converged on a solution, the flight of the ion was simulated with a separation simulation program. In practice, an ion has successfully shuttled through the junction matching the simulation.

The ion height fluctuates by about 10 μm in the Roadrunner but this is similar to the variation in the HOA trap [1]. To minimize the axial psuedofield, the ion needs to vary in height in the junction region. Though seemingly large, the variation is small enough that the ion can be shuttled through the junction. Holding an ion in the junction is a little more tricky as the rf node is poorly defined, so moving through it is preferred. Additionally, the variation in the axial pseudofield is 5 meV in the Roadrunner and 1 meV in the HOA. In both cases, the variation is 1000× larger in the junction than in the center region of the trap. From this comparison, we can conclude that the junctions are very similar in the two devices other than the opening angle.

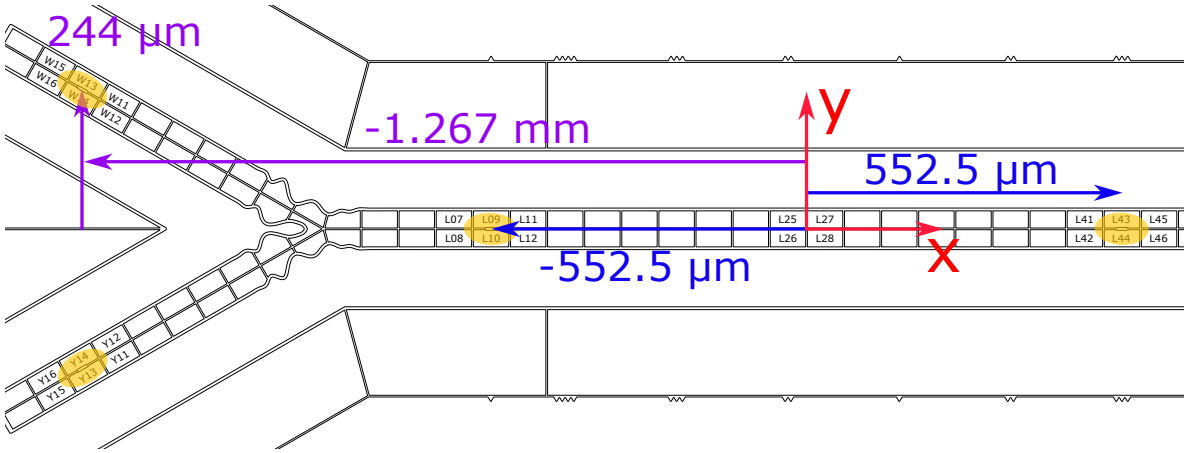

Figure 2-6.: Schematic of the Roadrunner Loading Hole Locations: The location of the center of each loading hole with respect to the origin is identified in the image, highlighted with yellow to guide the eye. The holes for loading near the quantum region are aligned to the trap axis in y, thus only the x position is given. In the junction, the loading holes are symmetric about the x-axis.

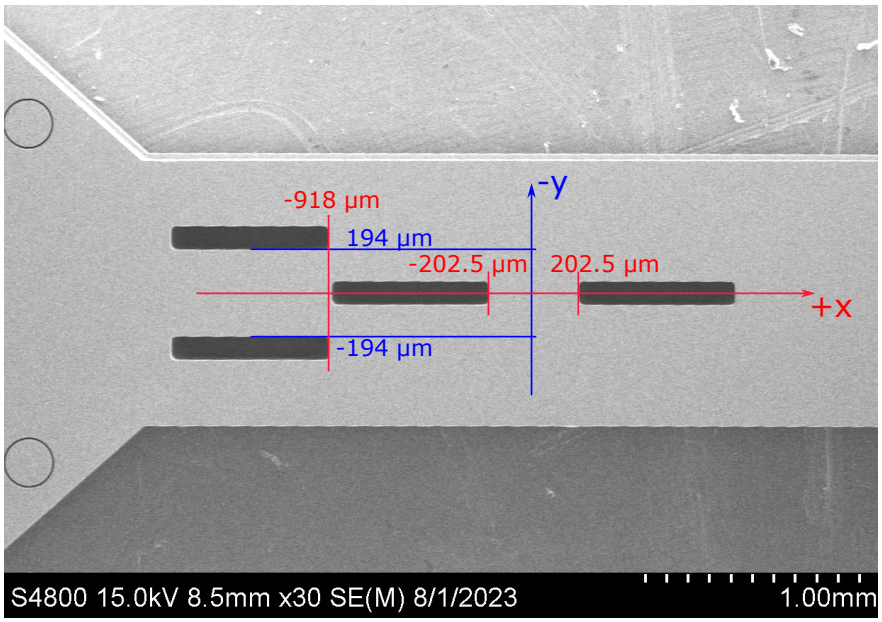

Figure 2-7.: SEM of the Roadrunner Backside: The hole through the handle silicon of the trap allow for atomic beams that were previously used for an HOA or a Phoenix/Peregrine trap to align to at least one of the loading holes in the Roadrunner trap. Each backside hole is 100 µm by 700 µm in y and x respectively. The location of each slot with respect to the origin is identified in the image (to see the backside, the trap has been rotated around the trapping axis, hence the reversal of the y-axis. The holes for loading near the quantum region are aligned to the trap axis in y, thus only the x position is given.

2.5. Loading Regions

This trap has several loading holes thus enabling a variety of loading locations. Each loading hole has the same dimensions and moderately backwards compatible with previous trap designs due to the number of holes. The backside hole is not centered on all of the front side holes to help with backwards compatibility, by increasing the opening angle of the backside towards ovens that would have been aligned to a Phoenix/Peregrine or HOA traps. There are two loading holes in the legs of the trap which are -1.267 mm in x and 244 µm in y from the center of the trap. The two loading holes in the linear region of the trap (L electrodes), are each 552.5 µm from the center in the x axis, but are aligned to the center in the y axis.

Each loading hole is mostly hidden in the gap between the electrodes thus causing a minimal amount of perturbation to the pseudopotential. Each loading hole has the same overall dimensions 20 µm by 5 µm in the top metal and the locations on the trap are given in Fig. 2-6. However, the limiting aperture of the loading hole is 1 µm by 17 µm and centered on the hole in the top metal, this is in metal layer one (M1), shown in Fig. 5-1. This smaller aperture limits the exposure to dielectrics in the loading slot. The backside silicon (see Fig. 2-7) has an expanded slot to allow for a larger acceptance angle for loading. The details of the backside positions are in the figure to allow for calculating the angle to a user's specific oven configuration.

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3. CONTROL SOLUTION GENERATION

To generate voltage solutions, a solved boundary model is needed. This is generally created from a meshing of the trap under consideration. The solved boundary element model is typically saved in a '.bec' custom format binary file. There have been no changes in file format since the previous QSCOUT trap, the Peregrine. For information on creating voltage solutions, see the Phoenix and Peregrine Manual Ref. [2].

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4. TRAP FEATURES

4.1. Optical Access

The High Optical Access (HOA) trap platform was designed to accommodate tightly focused laser beams across the surface of the trap in order to achieve high laser intensities at the ion positions and to enable individual addressing of ions in a chain. Sandia first introduced this platform in the similarly named HOA trap [1], and is discussed in detail in the HOA manual.

The optical access is parameterized by the open angle between the ion and the trap or package surface. The vertical NA is about 0.11 since the ion is 68 µm above the trap surface and the limiting aperture is the edge of the trap (0.6 mm in y). In the case of the Roadrunner trap, both the trap and the package impose similar restrictions on the solid angle across the surface of the trap. The vertical numerical aperture (NA) for a beam passing parallel to the trap surface is limited by the isthmus of the trap. The ion sits in the rf node 68 µm above the surface. The width of the isthmus of the trap (the width of the bowtie at its narrowest) is 1.2 mm, just as in the HOA and Peregrine trap. Thus, NA is 0.11 for a beam propagating perpendicular to the isthmus of the trap, and 0.08 for a beam propagating at 45°. As the minimum and maximum possible beam radii depend on propagation direction and wavelength, we do not offer a size limit. However, we recommend maintaining a separation between the surface and the propagating light of 3× the beam waist at all points above the trap (not just the center).

4.2. Rf Probe

The stability of the rf voltage on the device is paramount for creating stable radial modes. While the rf reflected from the device or transmitted to the device are a reasonable proxy for the voltage at the trap, there can be sources of variation that these do not account for.

Additionally, the current method for accurately determining the voltage applied to the trap is to measure the radial frequencies of the ion and compare to the trap model. However, if an ion has yet to be trapped in the device, the voltage is estimated based on the previous devices or estimated rf losses in the system. Inaccuracies in the estimate can lead to far exceeding the desired voltage or trying to trap with too low of an amplitude. Knowing the applied voltage more precisely in advance of trapping an ion can reduce the uncertainty in trying to trap.

In the Roadrunner trap, an rf sense wire is present to allow measurement of the rf voltage on the device. The rf sense is capacitively coupled (C≈0.024 pF) to the rf trace via an approximately 600:1 capacitive divider. Our bench measurements of an S21 on a single Roadrunner showed -56dB at 80 MHz. Some variation across devices and for different frequencies is expected. However, this

probe, once calibrated, is an accurate indication of the rf voltage on the device and can be used as part of a feedback circuit to stabilize the rf voltage on the device.

4.3. Resistive Wires for Heating or Temperature Sensing

Cryostats have a limited heat load capacity and while we can calculate the expected heat load of a trap, this may vary from device to device. Knowing the temperature of the device during operation may help tune the rf and to optimize heat dissipation through the cryostat. Additionally, keeping the trap at a higher temperature than its surrounding while cooling the cryostat may prevent condensation on the trap surface.

Towards that end, we have incorporated a heater and temperature sensing wires into the trap. While the benefits of these wires are clear in a cryogenic setting, they can also be used in room temperature.

There are two sets of wires in the trap, one aluminum and the other made from tungsten (Heater). In Table 6-2, the aluminum wire is listed as 'Tsense' and is located on the M1 metal layer (see Fig. 5-1). The 'Tsense' wire has a lower voltage limit as it is connected to trench capacitors in the device and thus is limited to voltages of < 20 V and currents of 2.4 mA, same as the electrodes. However, the trench capacitors will limit the rf pick-up on the wire, thus making it ideal for measuring the temperature. The entire wire should have a resistance of about 510(5) Ω. Due to slight variations from device to device in the metal and dielectric thicknesses, giving an accurate equation for the calibration of this wire is not possible. However, this can be calibrated for a specific device. Without applying rf to the trap, we mapped the temperature to the resistance of a similar wire from a Phoenix trap in a cryostat while cooling. At high temperatures (room temperature), the resistance vs temperature response is nearly linear (very approximately 10 Ω/K) and as it approached 4 K, the resistance begins to flatten out around 80 Ω.

The tungsten wire (labeled as 'Heater' in Table 6-2) is not connected to the integrated trench capacitors and thus can be operated at a higher voltage. Since it will be more susceptible to rf pick-up, this wire is more suited for heating the device. The room temperature resistance of the tungsten wire is approximately 4.2(2) kΩ and should decrease at lower temperatures. Additionally, tungsten does not suffer from the same electromigration limit as aluminum and should be limited by the wirebond and dielectric breakdown. For these wires, the voltage and current limits are 100 V (either dc or rf) and 0.4 A. The higher current limit of the tungsten allows for greater heating capacity and is recommended for use as the primary heater (should one be used).

4.4. Rf Dissipation

Having a large rf dissipation on the trap can lead to undesired heating of the device. Both the resistance and the capacitance of the Roadrunner have been reduced as much as possible to minimize dissipative loss. This was accomplished by keeping the junction near the center of the

Table 4-1.: List of the measured capacitance (C_p) and the series resistance of the rf trace (R_s) on the trap (package not included in measurement). The dissipated power (P_s) is calculated from these measurements. The measurements from previous devices is left for comparison.

Trap	C_p	R_s	P_s
Roadrunner	5.1 pF	1.0 Ω	53 mW
Peregrine	3.8 pF	0.7 Ω	20 mW
Phoenix	4.9 pF	0.6 Ω	30 mW
HOA-2.1	7.6 pF	0.9 Ω	100 mW

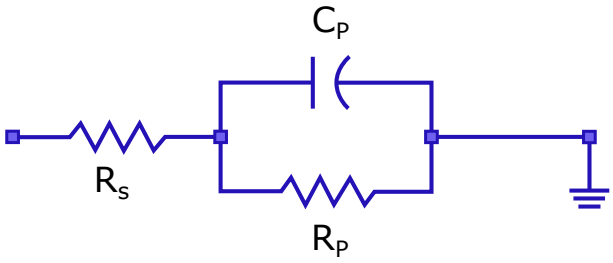

Figure 4-1.: Schematic of the approximate rf circuit diagram. R_s is the series resistance, resistance from the rf lead. R_p is the parallel resistance, loss from dielectric absorption. C_p is the parallel capacitance, the capacitance from the rf trace.

isthmus and keeping the legs short. The power dissipated (P_s) in the trap at a particular rf drive frequency (ω) can be approximated from:

$$P_s = \frac{1}{2} R_s U^2 \omega^2 C_p^2 \propto L^3, \; P_p = \frac{1}{2} \frac{\omega U^2}{R_p} << P_s. \tag{4.1}$$

where R_s is the rf series resistance, C_p is the parallel capacitance of the rf, U is the potential on the rf, and L is the rf length. Figure 4-1 shows the electrical schematic of the rf that defines the capacitance and resistance. The resistive loss of the rf dominates over the absorptive loss (P_p) from the dielectric. To minimize this loss, we should minimize L by keeping the rf feed and electrode as short as possible.

The measured resistances and capacitances are shown in Table 4-1 along with the estimated power dissipation compared to the HOA-2.1, the Phoenix, and the Peregrine traps. The addition of the junction and the longer quantum region in the Roadrunner trap are the main contributors to the higher heat dissipation. The width of the rf was optimized based on the ion height and is thus comparable to previous traps. However, the length of the trap was chosen to minimize the rf length while keeping a large quantum region. The rf feed is symmetric and from a single end minimizing the length and consequently, the capacitance.

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5. TRAP FABRICATION

The delivered devices contain the following materials:

Device Silicon, silicon dioxide, silicon nitride, aluminum, copper, titanium nitride, titanium, platinum, tungsten, gold.

Die attach Au80Sn20 solder, EpoTek H21D, or SAC solder (as specified in the device specific documentation – PowerPoint presentation sent with the device).

Package Aluminum Nitride, Gold, Nickel, Tungsten. Pins (optional): iron, nickle, and cobalt alloy and silver-copper braze.

5.1. Trap Chip

This device was fabricated using 6 metal levels (Figure 5-1); the top (M6) is the electrode level and the lower metal layers (M1, M2, M3, and M4) are used for routing control lines. The penultimate layer (M5) is reserved for ground metal to shield the dc electrode routing from the rf. In locations where metal below the electrodes is exposed to the ion (such as M5 between the M6 electrodes), the exposed metal is grounded. AlCu (99.5%/0.5%) is used for the metal levels, with tungsten vias for vertical interconnections. All electrodes are overhung from the underlying silicon oxide insulating layers. Unless otherwise specified, the top metal is over-coated with 250nm of gold, using 100 nm of titanium and 100 nm of platinum for adhesion.

5.2. Package and Die Attach

These devices are packaged on top of a high-temperature co-fired ceramics (HTCC) Aluminum Nitride custom bowtie shaped package integrated onto either a ceramic pin grid array (CPGA) or ceramic land grid array (CLGA) Figure 5-2 or 5-3 show the differences between the two packages. The trap is attached on top of the package using solder (Au80Sn20 or SAC305).

The Au80Sn20 solder is jetted onto solder pads on the ceramic package using a solder jetter. The bottom of the die has matching solder pads and the die is placed and the solder is reflowed in nitrogen or formic acid using the Finetech Femto 2 die bonder.

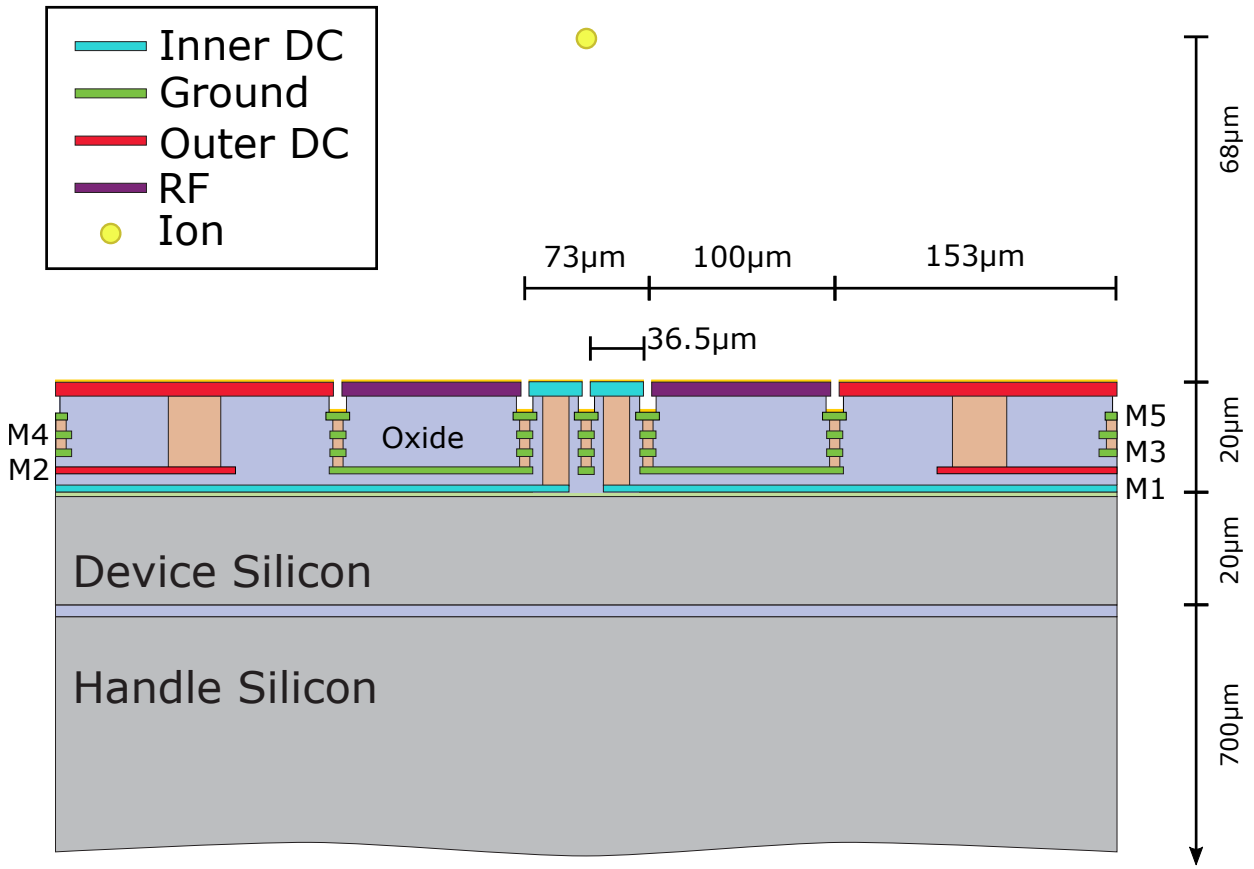

Figure 5-1.: Cross section of the Roadrunner trap. (Not to scale.) This image shows the important distances of the electrodes, and ion, as well as the overall trap thickness. Starting from the bottom, the handle silicon is 700 µm thick and makes up the majority of the trap thickness which comes from the wafer begin used. On top of the handle is device silicon, which we manufacture the trench capacitors into. The trap is fabricated using a 6-metal-layer process and a cartoon of each layer is shown on top of the device silicon. All of the control electrodes are located on the same layer, top metal, where the routing takes place underneath, shielded from the rf by ground metal. The ion is about 68 µm above the electrodes in the center of the linear region. All of these thicknesses are nominal and vary slightly from trap-to-trap.

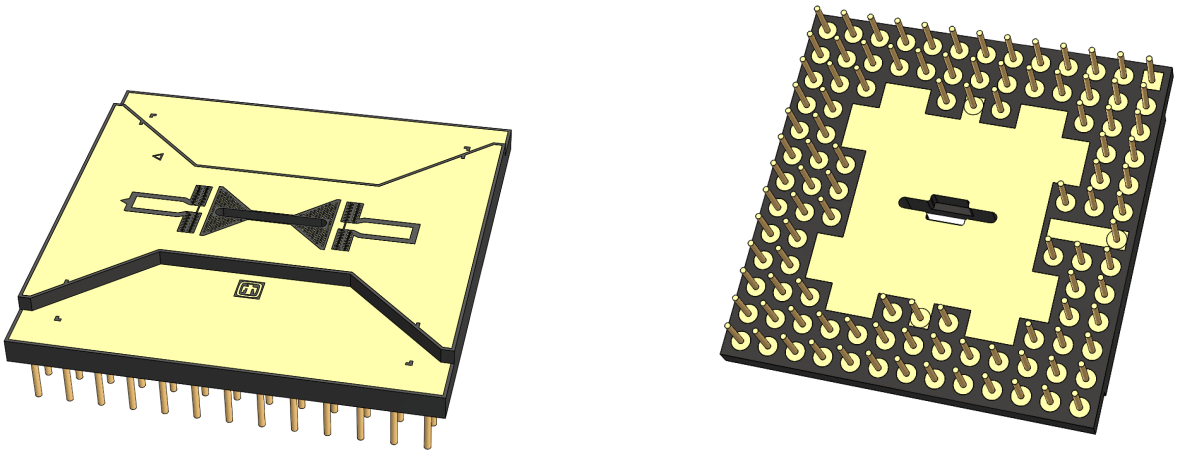

Figure 5-2.: Renderings of the CPGA package. The bowtie shape preserves the optical access to the isthmus region of the trap. All metal surfaces of the package are electrically connected to one or more pins (no floating metal). The small triangle located in the upper left corner of the package bowtie marks the rf feed direction of the device as does the small triangle tab on the rf trace (center left on the package).

We recommend a maximum baking temperature of 200°C for less than 7 days to achieve ultra-high vacuum. Though, this guidance may be updated for longer bakes in the near future, so the details should be verified for a particular device. This maximum temperature and time mitigate the formation of brittle and high resistivity gold-aluminum inter-metallic at the wire bonds. We have exposed the trap to a maximum temperature off 225°C for the vacuum bake and therefore do not recommend exceeding this value for any length of time. The glass transition temperature is 240°C and the glass melting point is 370°C, so in principal the trap could go much higher. However, higher temperatures risk accelerating the formation of a gold-aluminum inter-metallic that degrades the wirebonds, so the maximum bake time at higher temperatures is much shorter pending the change to include gold on the bondpads.

The metal routing in the package is 10 µm thick tungsten. The package surface is gold coated, where the thickness of the metal plating is 2.5 µm gold minimum on 1.27 µm Nickel minimum. Aluminum nitride ceramic was chosen, instead of alumina, because of its higher thermal conductivity to more closely match the thermal expansion properties of the silicon device.

5.3. Wirebonding

Wirebonding locations are optimized for beam access. There are no bondpads down the center isthmus of the trap to allow access for laser beams. The trap chip bondpads are located on the long ends of the bowtie and are 95 µm wide with a 5 µm gap to each neighbor. Both the control electrodes and the rf are wirebonded directly to the package. To allow for higher voltages, the rf is connected to the package with 7 wirebonds, as opposed to the control electrodes, where only 1 wirebond is used. Fig. 5-4 shows images of the low profile wirebonds near the rf feed of the trap.

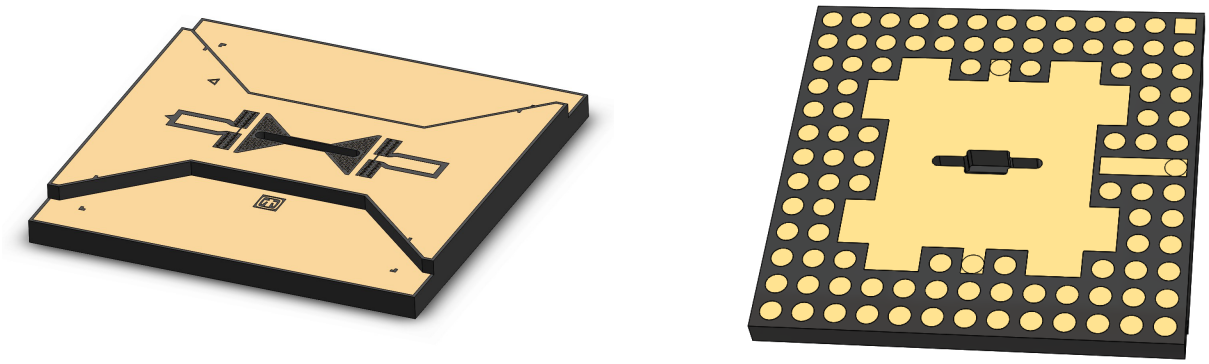

Figure 5-3.: Renderings of the CLGA package. The top portion of the package is the same as the CPGA package, but the backside has lands instead of pins. All metal surfaces of the package are electrically connected (no floating metal).

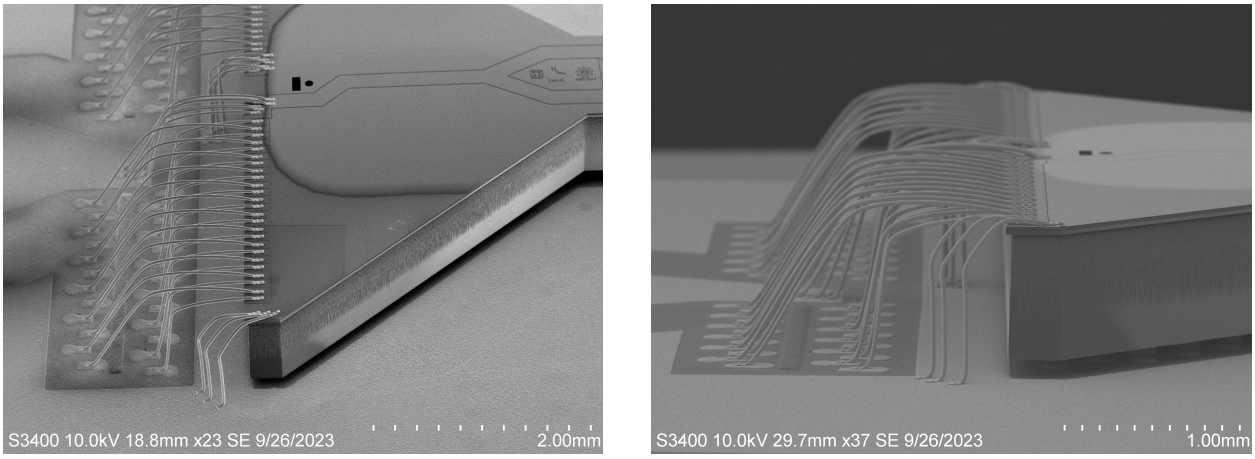

Figure 5-4.: (Left) Scanning electron micrograph of the wirebonds on a Roadrunner trap chip to the package as seen from above. Wirebonds connect all the dc control signals from the trap directly to the package. The rf electrode is connected with 7 wirebonds to keep the capacitance as low as possible. There is a gap in the wirebonds at the center edge of the device to allow a beam to pass over the isthmus unobstructed. The kink in the rf electrode path on the far left moves the rf off the centerline at the edge of the trap to allow for this gap. (Right) Side view of the Roadrunner wirebonds. The bonds are very low profile to keep wires out of the diagonal beam paths as much as possible.

5.4. Testing

Before delivery, the packaged traps are tested for shorts between every combination of electrodes. The capacitance is measured from every control electrode to ground as a test of the integrated trench capacitors. Using a charge induced image contrast technique with an SEM, the electrode connections are verified, testing the possibility that a disconnected wirebond or internal via leaves the electrode floating. The rf electrode resistance is measured to ground with a separate multimeter to ensure that it exceeds 40 MΩ. Finally, the device is inspected optically to ensure no surface contaminants are present on the trap which would interfere with trap performance.

The results of these tests are documented and shipped with the devices which are labeled with a unique designator on the package surface that also provides internal information regarding the specific wafer and fabrication steps, as well as the photomasks used in fabrication.

If any non-standard features are present (such as wirebond jumpers or additional capacitors), it will be detailed in the part-specific testing documentation.

The devices are maintained in a cleanroom environment throughout their assembly. After final electrical testing they are plasma cleaned, with an argon plasma treatment for 5 minutes at 10 Watts, then stored in a package and placed in an antistatic bag for shipment. Installation of the device should occur in as clean an environment as possible to prevent contamination (preferably a clean room) and as soon as possible upon receipt.

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6. THE BOWTIE-102 PACKAGE

The Roadrunner is packaged on a custom designed HTCC package. This custom package was originally realized for the Phoenix and Peregrine traps to improve performance and simplify the trap packaging process, and we continue to use an updated version with lower resistance due to the good performance.

The package is available with and without pins as a CPGA) and as Ceramic Land Grid Array Package (CLGA), respectively. A rendering of the CPGA package is shown in Figure 5-2. Figure 5-3 shows the land grid array package. The package offers high thermal conductivity, low rf trace resistance, and many grounding paths through the package. To realize good thermal conductivity, the package is fabricated from aluminum nitride (AlN). Superior rf resistivity is achieved by routing the rf trace on the outside of the package where good conducting materials are available. The necessary vias are massively parallel to reduce resistivity. All exposed metal on the top and bottom of the package that is not a control signal, is connected to ground. Close attention was similarly paid to the routing of the rf ground to reduce the resistivity of the rf return signal. The mechanical dimensions of each package can be found in Figs. 6-1 and 6-2, for the CPGA and CLGA, respectively.

The resistance and capacitance of the rf trace were measured to be 40.8 mΩ and 2.9 pF, respectively.

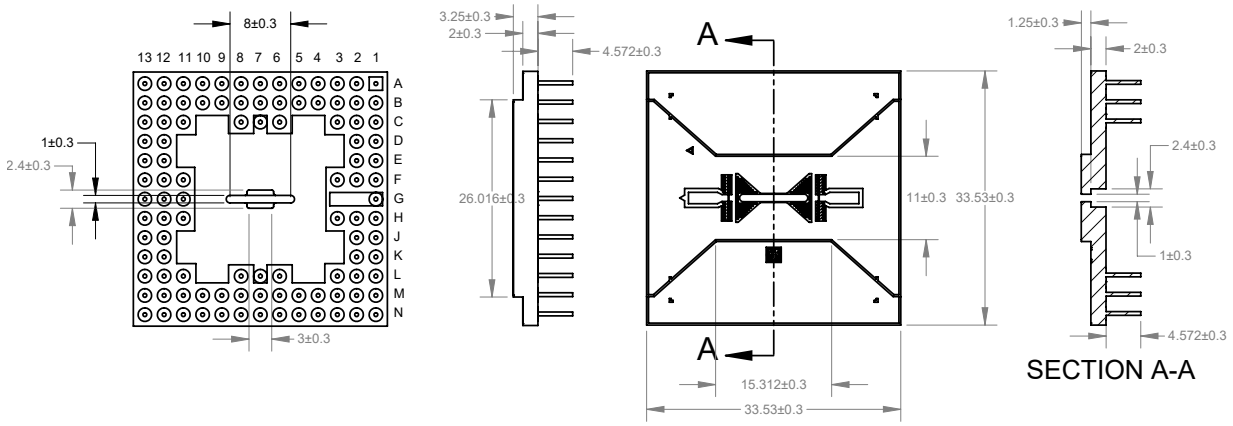

Figure 6-1.: Mechanical dimensions of the CPGA Bowtie-102 package. This is a section of the full package drawing which is available upon request. The dimensions are in units of mm.

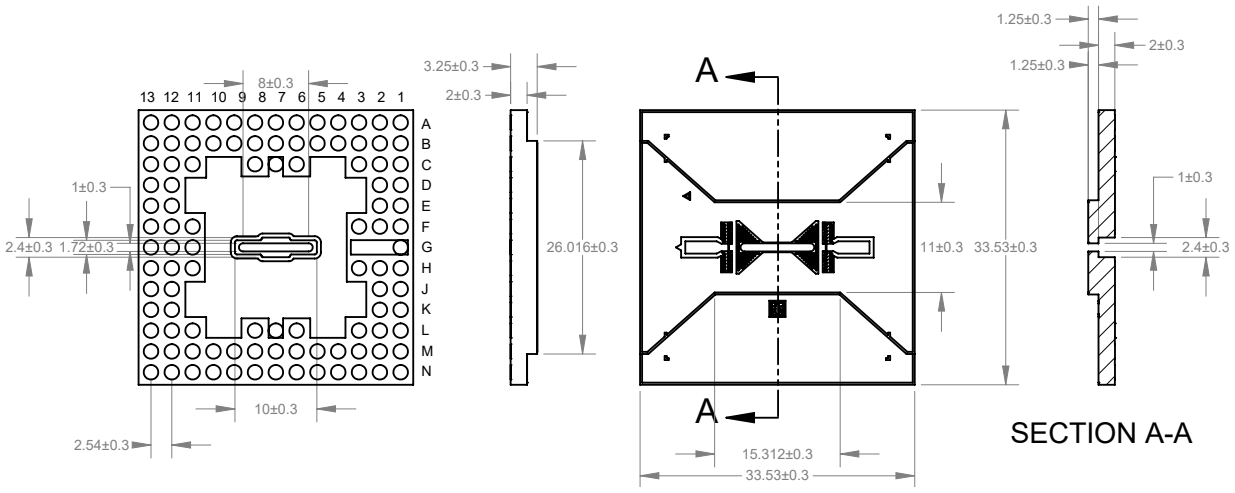

Figure 6-2.: Mechanical dimensions of the CLGA Bowtie-102 package. This is a section of the full package drawing which is available upon request. The dimensions are in units of mm.

6.1. Package Netlist

The CPGA package (Figure 6-3) has 102 pins and is identical to the previous CPGA package for the Phoenix and Peregrine devices [2]. There is one pin each for rf (G1), and secondary rf (G11) connections (see Fig. 6-4 for pin labelling), 2 ground pins at locations C7 and L7, and 98 control signal pins. To achieve lower resistance, the rf signal is routed at the outside of the package from site G1 through site G3. In the CPGA package the pins at sites G2 and G3 are omitted. In the CLGA package sites G2 and G3 can optionally be used for additional rf connections. In addition there are 16 additional locations that allow for ground connections at locations C4, C5, C9, C10, D3, D11, E3, E11, J3, J11, K3, K11, L4, L5, L9, and L10.

The bondpads on the front side of the package (ID-1 . . . ID-100) are labeled in Figure 6-4, and the package grid locations are labeled in Figures 6-1 and 6-2. These are connected according to the following Netlist in Table 6-1.

Table 6-1.: Netlist for the package grids (from Fig. 6-3 to the package bondpads (ID-1 . . . ID-100).

ID	Package Grid	ID	Package Grid	ID	Package Grid
ID-1	C3	ID-35	H1	ID-69	M10
ID-2	C7	ID-36	N3	ID-70	L13
ID-3	B2	ID-37	M1	ID-71	M7
ID-4	D1	ID-38	N6	ID-72	H11
ID-5	A5	ID-39	J1	ID-73	N10
ID-6	E2	ID-40	M3	ID-74	G12
ID-7	A2	ID-41	L2	ID-75	L8
ID-8	A1	ID-42	M5	ID-76	C8
ID-9	B5	ID-43	J2	ID-77	F11
ID-10	E1	ID-44	N2	ID-78	A10
ID-11	B3	ID-45	N1	ID-79	G13

Table 6-1.: Continued.

ID	Package Grid	ID	Package Grid	ID	Package Grid
ID-12	C2	ID-46	N5	ID-80	B7
ID-13	A6	ID-47	K1	ID-81	F12
ID-14	F1	ID-48	M2	ID-82	B10
ID-15	A3	ID-49	L7	ID-83	C13
ID-16	B1	ID-50	L3	ID-84	B8
ID-17	A7	ID-51	L11	ID-85	F13
ID-18	F2	ID-52	K13	ID-86	A11
ID-19	B4	ID-53	M12	ID-87	D12
ID-20	D2	ID-54	N13	ID-88	A8
ID-21	B6	ID-55	N9	ID-89	E13
ID-22	F3	ID-56	J12	ID-90	B11
ID-23	A4	ID-57	N12	ID-91	B13
ID-24	C1	ID-58	L12	ID-92	B9
ID-25	C6	ID-59	M9	ID-93	E12
ID-26	L6	ID-60	J13	ID-94	A12
ID-27	H3	ID-61	M11	ID-95	C12
ID-28	N4	ID-62	M13	ID-96	A9
ID-29	L1	ID-63	N8	ID-97	D13
ID-30	M6	ID-64	H13	ID-98	B12
ID-31	H2	ID-65	N11	ID-99	A13
ID-32	M4	ID-66	K12	ID-100	C11
ID-33	K2	ID-67	M8	RF	G1
ID-34	N7	ID-68	H12	RF2	G11

6.2. Trap on Package Netlist

In the following Netlist table, the Package grid locations are labeled in Figure 6-3 and the pad locations are in shown in Figure 6-4. The electrode names are described in Figure 2-1. The trap die contains 144 trench capacitors (2 are connected to each electrode and the 'TSense' wire). These capacitors are not all identical, so there are 3 different possible capacitances at the electrode. The capacitor value column in the Netlist (see Table 6-2 in Sec. 6) shows the expected capacitance for each electrode from calculations. These values are approximately what can be measured, the parallel capacitance of all capacitors connected to that electrode. Electrodes with a larger area are in general connected to larger capacitors.

The 'Tsense' wire is an aluminum wire located on metal one (M1) and is connected to two trench capacitors. At room temperature the resistance of this wire is approximately 510 Ω. See Sec. 4.3 for more detailed information.

The 'heater' wire is a the tungsten resistive wire and is located close to the silicon substrate but electrically separated from it (see Sec. 4.3). This wire follows the top perimeter of the trap die and

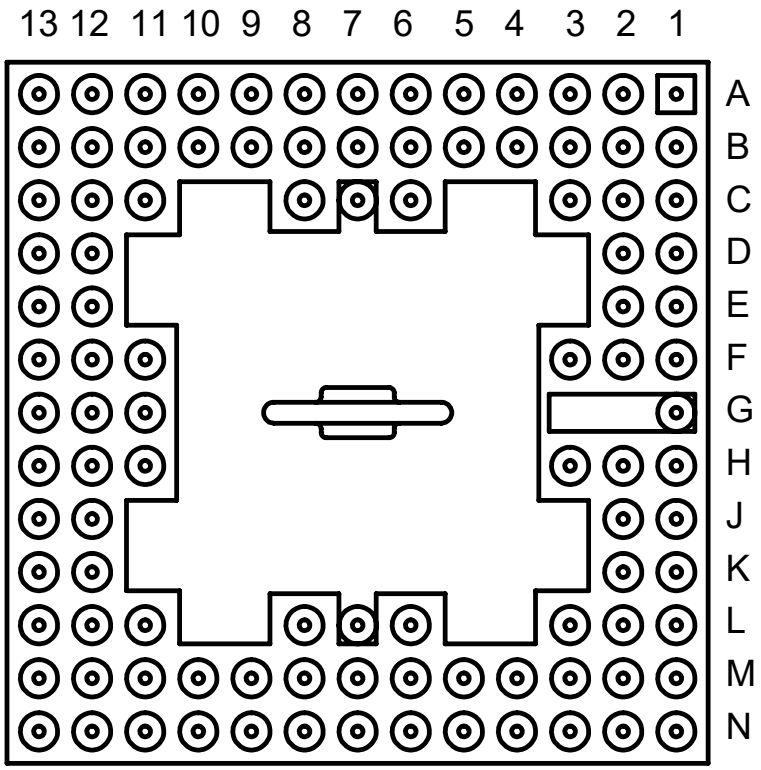

Figure 6-3.: Drawing of the CPGA Bowtie-102 package as seen from the backside. The main rf connection is at location G1. Sites G2 and G3 are also connected to the rf signal; however, these sites do *not* have a pin to enable usage in chambers designed for packages implementing the old MQCO packaging standard. This is seen in the drawing as the missing circles at G2 and G3, but the remaining rectangle is gold connecting the sites. Ground is at sites C7 and L7. Compared to the MQCO packaging standard, this package has 4 additional pins at locations C3, C11, L3, L11. These pins are used for resistive wires on the trap die.

Figure 6-4.: Package Pads. Numbering of the pads of the Bowtie-102 package. The package provides 100 control signal bondpads, two rf bondpads (RF1 and RF2) as well as a ground plane (not shown here).

can be used to either heat the substrate or to estimate its temperature. This wire is *not* connected to capacitors.

Table 6-2.: Netlist for the Roadrunner electrodes to the package pins (from Fig. 6-3). Each electrode is connected to two capacitors of differing values depending on the function of the electrode. The measured capacitance is given in the final column.

Package Grid	Electrode	Function	Capacitance (pF)
A1	A05	SIGNAL	536
A10	L25	SIGNAL	660
A11	L41	SIGNAL	660
A12	L15	SIGNAL	660
A13	L09	SIGNAL	660
A2	W17 W18	SIGNAL	536
A3	W11	SIGNAL	536
A4	A07	SIGNAL	755
A5	L03	SIGNAL	660
A6	W13	SIGNAL	536
A7	W16	SIGNAL	755
A8	L47	SIGNAL	660
A9	L11	SIGNAL	660
B1	GND	GND	0
B10	L33	SIGNAL	660
B11	A03	SIGNAL	660
B12	W01	SIGNAL	660
B13	L21	SIGNAL	660
B2	L07	SIGNAL	660
B3	W15	SIGNAL	536
B4	W12	SIGNAL	755
B5	W03	SIGNAL	536
B6	W08	SIGNAL	755
B7	L29	SIGNAL	660
B8	L37	SIGNAL	660
B9	L19	SIGNAL	660
C1	W04	SIGNAL	755
C11	Heater	Heater	0
C12	L13	SIGNAL	660
C13	L35	SIGNAL	660
C2	W07	SIGNAL	536
C3	Heater	Heater	0
C6	W02	SIGNAL	755
C7	GND	SIGNAL	0
C8	A01	SIGNAL	660
D1	L05	SIGNAL	660
D12	L45	SIGNAL	660

continued . . .

Package Grid	Electrode	Function	Capacitance (pF)
D13	J01	SIGNAL	660
D2	W10	SIGNAL	755
E1	W05	SIGNAL	536
E12	L17	SIGNAL	660
E13	L43	SIGNAL	660
E2	L01	SIGNAL	660
F1	W09	SIGNAL	536
F11	L23	SIGNAL	660
F12	L31	SIGNAL	660
F13	L39	SIGNAL	660
F2	W14	SIGNAL	755
F3	W06	SIGNAL	755
G1	RF	RF	0
G11	RF Sense	RF	0
G12	L24	SIGNAL	660
G13	L27	SIGNAL	660
H1	Y16	SIGNAL	755
H11	L28	SIGNAL	660
H12	L36	SIGNAL	660
H13	L46	SIGNAL	660
H2	Y08	SIGNAL	755
H3	Y02	SIGNAL	755
J1	Y07	SIGNAL	536
J12	L14	SIGNAL	660
J13	L22	SIGNAL	660
J2	A06	SIGNAL	536
K1	L06	SIGNAL	660
K12	L40	SIGNAL	660
K13	L10	SIGNAL	660
K2	Y12	SIGNAL	755
L1	A08	SIGNAL	755
L11	Tsense	Sensor	0
L12	L18	SIGNAL	660
L13	L32	SIGNAL	660
L2	Y05	SIGNAL	536
L3	Tsense	Sensor	0
L6	J02	SIGNAL	755
L7	GND	GND	0
L8	A02	SIGNAL	660
M1	Y09	SIGNAL	536
M10	L34	SIGNAL	660
M11	A04	SIGNAL	660
M12	Y01	SIGNAL	660

continued . . .

Package Grid	Electrode	Function	Capacitance (pF)
M13	L44	SIGNAL	660
M2	L08	SIGNAL	660
M3	Y15	SIGNAL	536
M4	Y10	SIGNAL	755
M5	Y03	SIGNAL	536
M6	Y06	SIGNAL	755
M7	L30	SIGNAL	660
M8	L38	SIGNAL	660
M9	L20	SIGNAL	660
N1	L02	SIGNAL	660
N10	L26	SIGNAL	660
N11	L42	SIGNAL	660
N12	L16	SIGNAL	660
N13	J03	SIGNAL	660
N2	Y17 Y18	SIGNAL	536
N3	Y11	SIGNAL	536
N4	Y04	SIGNAL	755
N5	L04	SIGNAL	660
N6	Y13	SIGNAL	536
N7	Y14	SIGNAL	755
N8	L48	SIGNAL	660
N9	L12	SIGNAL	660

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7. TRAP PACKAGING AND PARAMETRIC TESTING

Once the traps are mounted on the package, they can be parametrically tested for shorts and correct capacitance. The traps are also tested for connectivity between the trap electrodes and the pins or lands. The Roadrunner traps are solder die attached to the Bowtie-102 package using gold-tin (AuSn) solder. Introduction of this solder die attach process means that trap assemblies do *not* contain epoxies and are completely organics-free.

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8. TRAP INSTALLATION

The following describes the installation procedure for the user after receiving the trap.

Microfabricated surface traps are very sensitive to dust particles accumulated on the surface, as they can cause electrical shorts, accumulate static charges, and cause laser scatter. Therefore, we strongly recommend installing the traps *only in a cleanroom environment* to prevent contamination.

Additionally, the integrated trench capacitors can be damaged by static electricity or voltages above ±30V.

8.1. Vacuum Chamber

The user is responsible for building a UHV vacuum chamber to accommodate the packaged device. A chamber with 95 control voltages along with a dedicated RF and ground wired to be compatible with the package is necessary for the successful operation of the trap.

The success of the experiments will likely depend on achieving an excellent vacuum. All surfaces exposed to the interior of the chamber need to be handled in an absolutely grease-free way. Pressures below 10^{-10} mbar should be acceptable for many ion trapping experiments, although pressures significantly lower will result in superior trapping times (since the trap depth is only a few times room temperature).

The orientation of the trap in the vacuum chamber has an influence on the likelihood of getting dust particles located on the trap surface. If the trap surface is vertical or pointing down, dust accumulation on the surface is less likely.

Vacuum compatible zero insertion force (ZIF) sockets for the 100 pin CPGA package are available from Tactic Electronics (PN: 100-4680-001A).

8.2. Ground Plane Above Trap

The user is responsible for mitigating charge on nearby dielectric surfaces. Generally, the closest and most influential surface is the imaging viewport. While the package itself is not much farther away from the ion, the geometry limits the impact of charge that may build up on that surface (since there are many screening grounded regions between exposed dielectric of the package and the ion). The viewport, however, has direct line-of-sight to the ion and, unless mitigated, is mostly unscreened. Possible approaches include:

1. Building a custom metal screen which accommodates the necessary laser and imaging access and mounting this structure on the package. Screens with openings up to an NA of 0.6 have been operated successfully.
2. Coating the re-entrant viewport with a conductive transparent material (such as ITO)
3. Using a mesh with a small geometric fill factor.

In addition, the screen should be placed far enough away as to not have a significant impact on the electric field for an otherwise unscreened trap. If the screen is too close, it may cause the simulations of the electric field to be inaccurate. A good guideline is that if the distance of the screen to the trap surface is more than 20 times the distance of the ion above the trap surface ($\approx 68\,\mu m$), then the presence of the ground will have minimal impact on the trap behavior (in this case 1.4 mm is recommended). Above this minimum separation, the specific distance does not significantly affect operating conditions, such as the trap depth for a given rf voltage or the control waveforms. For screens closer than 1.4 mm, the voltage solutions may have to be adjusted for the presence of the ground screen.

8.3. Trap Insertion

These traps have to be installed with the gold tab on the package pointed in the direction of the socket's rf pins. The packages are quite robust and can be pushed in with a great deal of pressure, however the user should be careful not to touch the wirebonds on the trap and only contact the package surface and to remember that the package is still ceramic and can break if a mechanical advantage is used. Also, it is crucial to ensure that none of the pins are being bent while inserting the package into the socket. If the trap needs to be retracted and used again, care should be taken to not bend the package pins.

The traps have to be installed in a dust-free and clean environment, ideally a cleanroom, to limit the possibility of dust falling on the chip surface. If that is not feasible, they should be installed as quickly as possible to minimize exposure.

8.4. Pre-bake Testing

Before baking, the user should verify that the rf electrode is not shorted to ground and measure its capacitance. The capacitance of the packaged device should measure as 8 ± 1pF, the bare die is 5 ± 1pF, and 3 ± 1pF for the CPGA carrier. These values do not include the capacitance of the feedthrough and socket (which depends on the wiring but is $\approx$ 6pF in our chambers) and should be measured by the user before device insertion.

If higher than normal dc voltages are to be applied, they should be tested at high vacuum before baking to make sure the device can handle them. During testing, dc voltages should be applied through a large resistor to limit the current, and any leaking current should be measured with a picoamp meter. In this setup, a rising current is indicative of a voltage close to breakdown.

The user should also verify that all dc control electrodes are not shorted to ground and measure their capacitance; if the capacitance does not match the expected value and the wiring harness is known to be correct, then the electrode is likely shorted to a neighbor (either on the chip or in the wiring of the vacuum chamber).

8.5. Baking

The devices themselves can be baked up to 200°C, limited by the die attach and the development of purple plague [6]. It may be the case that other components (such as Kapton wires) in the vacuum chamber limit the bake to a lower temperature.

As described in section 5.3, the device is packaged using wirebonding with gold wires connected to aluminum pads. If this junction is heated, brittle aluminum-gold intermetallics are formed. The aluminum-gold intermetallic will lead to a reduced pull strength, and more importantly, a slightly higher contact resistance of the wirebonds. A higher contact resistance can impact the rf dissipation and lead to a run-away affect of purple plague formation and can shorten the device lifetime. This process depends strongly on the baking temperature (see Fig. 2 in [6]), thus limiting the baking time when using high temperatures is most effective in preventing the formation of purple plague. Our tests show that baking of up to 7 days at 200°C is acceptable. We are continuing to advance the packaging of new devices and may soon have traps with longer bake times available. Questions or concerns should be addressed upon receipt of the device.

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9. TRAP OPERATION

9.1. Rf Voltage Application

(All capacitance values are estimates and subject to change between devices.) The Roadrunner devices have a total capacitance between rf high and ground of ≈ 8 pF, including the package (which adds 3 pF). In an ideal quadrupole trap, the trap secular frequency is given by:

$$\omega_{\text{sec}} = \frac{qV}{\sqrt{2}\Omega_{\text{rf}}\, mR^2},$$

where q is the charge of the trapped particle, V is the voltage amplitude, Ω_{rf} is the applied rf angular frequency, m is the mass of the particle, and R is electrode distance. This can be simply modified to calculate the secular frequency in the trap by substituting R for the characteristic distance of the device. The characteristic distance corresponds to the distance at which hyperbolic electrodes operating at the same voltage and frequency would generate the same secular frequency as in the surface trap. The characteristic distance for the Roadrunner trap in the slotted region is:

$$R = 126\,\mu\text{m}.$$

By substituting R with this number, the user can calculate the secular frequency they are generating for a particular voltage, drive frequency, and ion species, such as the plots shown in Fig. 2-2.

The trap depth can be expressed as:

$$d = \alpha\frac{1}{2}m\omega_{\text{sec}}^2 R^2, \quad \alpha = 0.028,$$

where the factor α is required to account for the specifics of the surface trap geometry. In terms of practical trap depth (defined as the ability to stay trapped following a collision with a particle of energy E), the stability parameter h also must not exceed 0.5 as that will prevent stable trapping even with a deep trap.

9.1.1. Rf Voltage Limit

The vertical separation between rf and ground in the Roadrunner trap is 4.7 μm. This decrease in separation as compared to the HOA trap has decreased maximum safe voltage to approximately 220 V. The maximum safe voltage, however, is dependent on the thickness of the gold applied to the trap and may vary from device to device. The safest practice to prevent potential damage to the device is to set up a monitor of the rf back reflection according to our methods in this paper [7]. The voltage should only be increased by about 25 V every thirty minutes until the desired maximum is

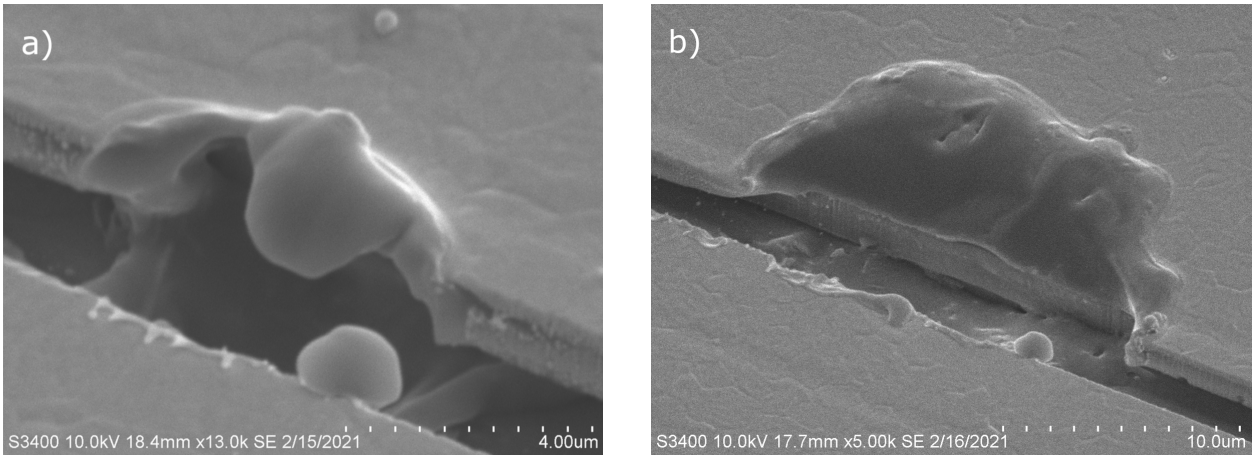

Figure 9-1.: (a) SEM of an rf rail on a Phoenix trap after a short has developed. (b) SEM of the same RF rail location after removing the short. The scales are different in the two images. Before removing the short, the metal disturbance is small, but a filament has formed connecting the rf to the ground plane below. After using current to remove the short, the filament is disconnected, but there is a large region of the overhanging electrode that has been blown upwards, disturbing the rf potential in the area.

reached. If the user needs to push beyond 220 V, this can be done with some risk, by monitoring. It should be noted that the Roadrunner trap has been designed to offer a deeper and tighter trap with lower voltages, so the 220 V limit can result in a 3.5 MHz radial confinement when using a 40 MHz drive frequency.

While studying this breakdown mechanism, there are typically many arc events that leave visible evidence, but shorting the rf is rare. Shorting occurs only at high voltages where the metal becomes molten and is thrown off by an arc, as seen in Fig. 9-1. This arcing is not correlated to the ion trapping location (as far as we can tell). The probability of disturbing the metal at the trapping site is no higher than anywhere else. Once the first breakdown event is observed, it is important to first lower the voltage and continue to monitor. The voltage can be increased again gradually, but if several breakdown events occur, the user is probably operating the device at too high an rf voltage.

9.1.2. Remove a Short

If the trap does develop a low resistance short (typically 1.5 Ω measured with a standard multimeter), the short can often be successfully melted away. We have had three instances of shorting on devices that are still being used to trap ions. In each case, we removed the rf resonator and attached dc leads directly to the rf and ground. We slowly increased the current going through the rf until we reached approximately 0.5 A. At this point, the filament melted and the short opened. Afterwards, the device was able to trap again and returned to normal operation. As long as the rf voltage was kept below the safe running limit from Sec. 9.1.1, we have not developed additional shorts. However, the removal of the short is about as violent to the trap as developing it, see Fig 9-1b. The metal that is melted away can also eject larger pieces, resulting in disturbing the rf potential such that the node is no longer stable. Removal of shorts is a last resort and developing a short should be seriously avoided.

9.2. Control voltages

Dc control voltages up to ±20 V are safe. The Roadrunner trap has a ±30 V breakdown limit for each control channel. Exceeding this limit is likely to result in the trench capacitor for that channel shorting to ground.

The trench capacitors are necessary to shunt rf signals (which couple via the parasitic capacitance between the rf electrode and the control electrodes) to ground. The trench capacitors are incorporated directly into the trap chip for each control channel and with a value relative to the size of the electrode as given in Table 6-2. The stray inductance of the trench capacitors themselves, which can undermine the ability to shunt the rf off the control electrodes, is 0.05 nH, much smaller than the $\approx$ 1 nH inductance that the wirebonds between the trap and the interposer add. The series resistance of the trench capacitors (4 Ω) is comparable to the lead resistance of the routing between bondpad and electrode on the trap chip.

The Roadrunner traps have control in the quantum region from segmented inner electrodes and a junction with independent arms. The schematic in Fig. 2-1 shows the electrode layout for the Roadrunner device. The rf trace is coming from the left, defining the orientation of the device. The orientation can also be determined from the triangle on the package (see Fig. 5-2 and 5-3) which is located on the left of the package with the rf feed and points towards the feed direction.

Tables 6-1 and 6-2 list the mapping between the electrode labels for the Roadrunner trap, the corresponding ID's, and the package grids. These tables should be combined with the wiring netlist for the particular vacuum system in use for trapping to generate the electrode-to-control channel netlist.

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10. ELECTROSTATIC SIMULATION

10.1. Trap Simulations

Boundary element simulations are employed to calculate the charge on all trap electrodes. From the boundary element solutions, the electrostatic potential $U_i(\mathbf{x})$ at location $\mathbf{x}$ generated by an electrical potential of 1V on electrode i while all other electrodes are at ground potential is calculated. Using the superposition principle, the potential generated by any set of voltages on the trap electrodes can be calculated from the set of U_i potentials. In addition, the ponderomotive potential generated by the rf electrodes can be calculated using

$$U_{\text{pond}} = \frac{eV_{\text{rf}}^2}{4m\omega_{\text{rf}}} \nabla U_{\text{rf}} \cdot \nabla U_{\text{rf}},$$

where e is the electron charge, V_{rf} the voltage amplitude of the radio-frequency drive, m is the ion mass and U_{rf} is the electrostatic potential generated by the radiofrequency electrode.

10.1.1. Voltage Arrays

The values of $U_i(\mathbf{x})$ are calculated near the rf nodal lines for all the electrodes and saved in a file. We call these data Voltage Arrays (`.va`).

File format The Voltage Arrays are saved in binary format and usually have a `.va` file extension. A file header giving information about the number of electrodes, boundaries, axes is followed by an array of potential values. The full file format is specified in Table 10-1.

Electrode assignment The voltage array files contain the potential for the electrodes in the order given in Table 10-2.

Type	Number	Content
64 bit Integer	1	
64 bit Integer	1	N_{elec}: Number of electrodes
64 bit Integer	3	n_x, n_y, n_z: Number of samples along the x, y and z axis
64 bit Integer	1	Number of voltage sets (1)
64 bit double	3	Re-mapped x-axis
64 bit double	3	Re-mapped y-axis
64 bit double	3	Stride along x-, y-, and z-axis
64 bit double	3	Origin
64 bit Integer	2	
64 bit Integer	N_{elec}	Electrode mapping
64 bit double	$N_{\text{elec}} \cdot n_x \cdot n_y \cdot n_z$	Potential data

Table 10-1.: File format of the binary voltage array files. (Any file ending in '.va') included as attachments, available upon request.

Index	Electrode
1	Ground
2	rf
3 . . . 10	A01 . . . A08
11 . . . 13	J01 . . . J03
14 . . . 61	L01 . . . L48
62 . . . 79	W01 . . . W18
80 . . . 97	Y01 . . . Y18

Table 10-2.: One-based index (as used in Mathematica) of the electrodes of the Phoenix trap in voltage array files.

11. SPECIFICATIONS AND ABSOLUTE MAXIMUM RATINGS

Geometry	
Bowtie length	10 mm
Bowtie width	6.4 mm
Bowtie height	790 µm
Isthmus width	1200 µm
Isthmus length	3.48 mm
Loading hole aperture (top metal)	5 µm×20 µm
Loading holes limiting aperture	1 µm×17 µm
Number of loading holes	4
Backside loading hole width	700 µm
Backside loading hole height	100 µm
Rf Electrode	
Maximal voltage on rf electrodes	$\pm 250\ V_{pk}$
Capacitance of rf on device	≈ 5.1 pF
Capacitance of rf on packaged device	≈ 8 pF
Est. rf dissipation 100 V, 100 MHz	53 mW
Rf sense divider ratio (unloaded)	$^{.024\,pF}/_{60\,pF} \approx 240$
DC Control electrodes	
Maximal voltage on dc electrodes	±30 V
Trench capacitor max leakage current ±10 V	10 nA (non-ohmic)
Number of control voltages needed	95
Quantum region	
Length	20×65 µm = 1.54 mm
Inner control electrode pairs	20
Inner control electrode pitch	65 µm
Outer control electrode pairs	2
Ion height	68 µm
Junction	
Control electrode pairs in legs	96
Control electrode pitch	65 µm
Maximum variation in ion height	10 µm
Trench capacitors (all dc control electrodes)	

Capacitance	536 pF, 660 pF, or 755 pF
Series inductance	$\approx$ 50pH
Series resistance (20°C)	4Ω
Maximum voltage	±30V
Damage Threshold voltage	> ±32V
Optical	
NA skimming the surface perpendicular to trap axis	0.11
NA skimming the surface at 45° to trap axis	0.08
NA vertically through central slot (Phoenix)	0.25

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Ray Haltli	Matthew Blain	Susan Clark
Tipp Jennings	Matthew Delaney	Melissa Revelle
	Nick Jimenez	Ashlyn Burch
	Ed Heller	Matthew Chow
	Zach Meinelt	Craig Hogle
RF Engineering	Becky Loviza	Megan Ivory
Christopher Nordquist	John Rembetski	Daniel Lobser
Stefan Lepkowski	Eric Ou	Dan Stick
Tyler Liebsch		Jon Sterk
		Christopher Yale
		Jay Van Der Wall

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13. ATTACHMENTS

The files listed below supply additional information about the trap, trapping potentials and voltage solution generation.

File Name	Description
CLGA_kdnb9b88a.pdf	CLGA package datasheet
CPGA_kdpb9f92.pdf	CPGA package datasheet
Roadrunner_Netlist.accdb	Netlist formatted in Access database
Roadrunner_Schematic.pdf	Roadrunner trap schematic. 10:1 scale
Roadrunner_Model_2019.sldprt	Roadrunner trap Solidworks (2019) model
Voltage Solutions/	Sub-folder for voltage control docs
Roadrunner.nb	Mathematica File for generating local Solutions
TrapEvaluation-201609.m	Notebook with equations for .nb file
Roadrunner.json	Electrode Assignments file - .json format
RS1798_quantum.va	Voltage Array for linear trap region
RS1798_jct_up.va	Voltage Array for upper junction trap region
RS1798_jct_dn.va	Voltage Array for lower junction trap region
RS1798_jct_in.va	Voltage Array for inner junction trap region
RS1798_arm_up.va	Voltage Array for upper arm
RS1798_arm_dn.va	Voltage Array for lower arm

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