Improved polysilicon surface-micromachined micromirror devices using chemical-mechanical polishing

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ABSTRACT

Surface polysilicon micromachined micromirrors require ultra-flat surfaces for advance optical applications such as adaptive optics. This paper details the planarization of micromirrors using chemical-mechanical polishing. We show that the increase in topography is due to a high temperature anneal step downstream from the CMP process itself. Two process alternatives were investigated: (1) perform a CMP step after the high temperature anneal step, and (2) perform a CMP step on the final polysilicon mirror surface. Both process alternatives produced acceptable flatness requirements for micromirror applications.

Keywords: micro-optical components, micromirrors, planarization, chemical-mechanical polishing, CMP, adaptive optics. Optical MEMS.

1. INTRODUCTION

Micro-optical mirror elements have widespread applications in optical systems such as flat panel displays, optical interconnects, adaptive optical arrays, scanners, optical beam steering, etc.[1-7] Recently, silicon and polysilicon micromachining technologies have been applied to optical micromirror component fabrication. Advantages for an optical system are lower mass, lower operating power, compact design, and the potential for large arrays of micro-optical elements.

Micromirror devices can be designed to transmit light intensity with or without phase information. As the application becomes more complex, the quality of the mirror surface and the ability to reproduce desired wavefronts becomes more important such as with adaptive optics [8]. In its resting state, for example, a micromirror element should have a flatness of < $\lambda/10$ of the operating wavelength.

We have recently developed a 5 level polysilicon surface micromachining technology at Sandia National Laboratories which employs the use of chemical-mechanical polishing (CMP) to planarize sacrificial layers of oxide stacked between the polysilicon layers [9]. This process has been used successfully to fabricate complex mechanical devices, alleviating the problems associated with severe topography generated during patterning and etching of multiple layers of thick polysilicon layers. Although not originally intended for optical device applications, Michalicek, et al. utilized the baseline process to fabricate a "proof of concept" micromirror [10]. The novel mirror design incorporated positioning flexures, support beams, and address electrodes directly beneath the mirror itself, thus making the mirror element compact and more easily controllable. It was believed that the CMP process, without any modification, would minimize the unintentional embossing problem caused when the final polysilicon mirror layer is placed directly above previously patterned layers of poly (i.e. the final polysilicon mirror layer conforms to the underlying topography). Some of the results that Michalicek reported showed that the flatness of these devices measured a "peak-to-valley" inherent deformation due to underlying patterns of 175.5 nm, which was not acceptable for adaptive optic applications. The obvious question was whether or not CMP was capable of achieving the required flatness. The purpose of this paper is to report on the planarization aspects for micro-optical element fabrication using polysilicon surface micromachining technology. We demonstrate an improved process flow that meets the required optical flatness tolerances required for advanced micromirror devices.

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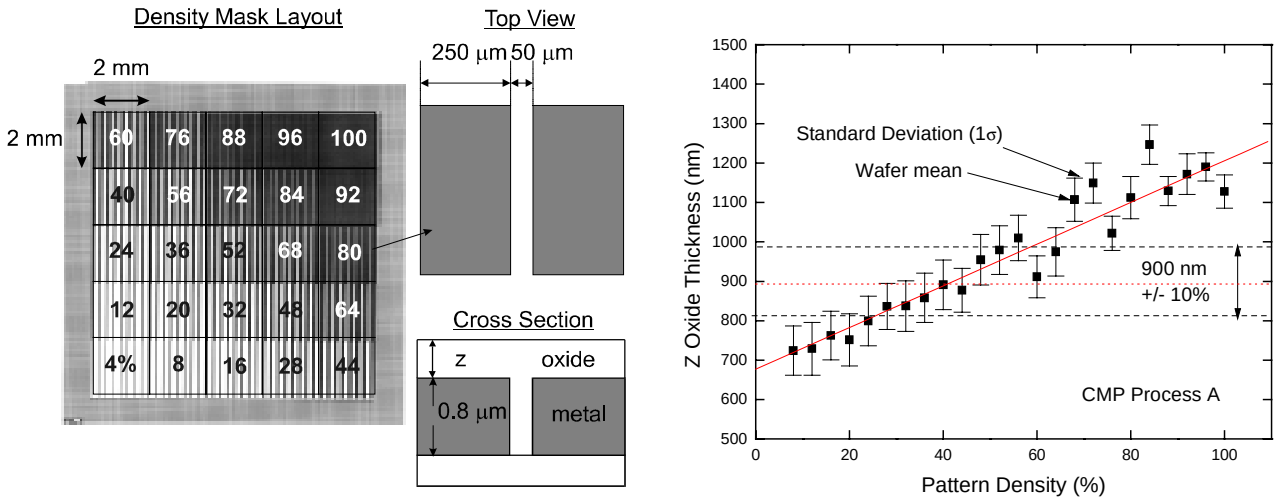
2. PLANARIZATION USING CHEMICAL-MECHANICAL POLISHING (CMP)

Chemical-mechanical polishing is a planarization process that can remove topography from oxide, metal, and polysilicon surfaces. CMP is the preferred planarization step utilized in sub-0.5 μm integrated circuit manufacturing. Many of problems associated with surface topography generated during fabrication, such as photolithography depth of focus budget, stringer generation during dry etch, and poor step coverage of metal layers during deposition are minimized or eliminated using polishing. CMP has also been utilized for fabrication of micro-electromechanical devices in order to remove the large step heights associated with the thick underlying polysilicon patterns [11]. Multilevel polysilicon surface micromachining with four or more layers is essentially precluded by the extreme topography generated unless CMP is used to reduce this topography.

A CMP process involves rotating a wafer against a polishing pad under pressure in the presence of slurry. In the Sandia polysilicon process, CMP is used to planarize intermediate layers of sacrificial silicon dioxide. For conventional oxide polishing, the slurry consists of a silica-based colloid suspended in a dilute alkaline solution (pH ~ 10-11). The polishing pad is typically a composite porous polyurethane-based material. The theory of oxide polishing is not well understood; however, it is generally accepted that the alkaline chemistry hydrolyzes the oxide surface and sub-surface thus weakening the SiO_2 bond structure [12]. The mechanical energy imparted to the colloid through pressure and rotation causes high features to erode at a faster rate than low features, thereby planarizing the surface over time.

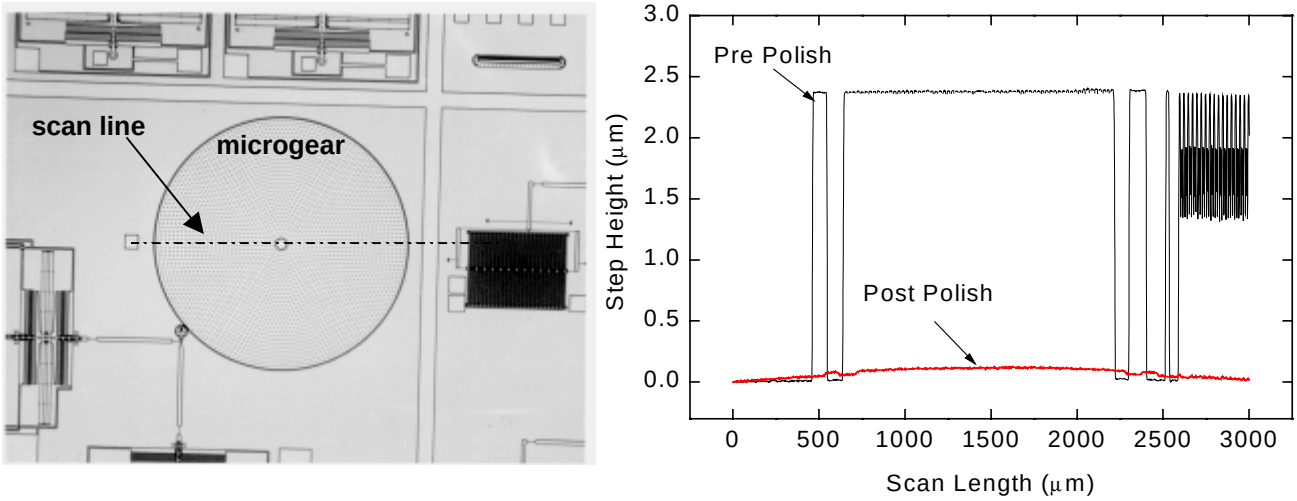
In developing a process flow incorporating CMP, consideration must be given to the pattern design layout, the incoming film type and associated step heights, and any downstream processes from CMP that may affect the overall planarity. It is well known that pattern density (the ratio of patterned area to the total area for a given length scale) affects the final die-level global planarity[13]. An example of this is shown in Fig. 1 where a CMP characterization test mask is used (Fig. 1a) to evaluate a CMP process. The test mask consists of patterns which vary in density from 4 % to 100 % for a given window size of 2 mm. The patterned wafers consist of a 0.8 μm thick metal pattern coated with a 2 μm thick oxide layer. After CMP, the oxide thickness over metal features within the die is measured and reported as a function of pattern density. As shown in Fig. 1b, the final oxide thickness over patterned features can vary significantly for a given CMP process and pattern density layout. For example, in targeting a final oxide thickness over the metal pattern of 900 nm +/- 10 %, the corresponding pattern densities range only between 25 and 60 percent for this particular process. This effect is due to the finite stiffness associated with the polishing pad as it conforms to topographic features on the wafer surface, the modulus of elasticity of the stacked films within the wafer, and the polishing parameters such as speed and pressure. A general rule of thumb is that wide, high-density patterns planarize the slowest and narrow, isolated features planarize the fastest.



(a) (b)

Figure 1. An example of a CMP characterization test mask used to evaluate the pattern density effect [13]. The mask layout is shown in Fig. 1a and the evaluation for a particular CMP process is shown in Fig. 1b.

A similar pattern effect for MEMs polishing is depicted in Fig. 2 where the initial and final surface topography of a microgear is shown. The initial step height is > 2 μm before CMP and is reduced to < 0.2 μm after CMP, which is acceptable for micro-mechanical



(a) (b)

Figure 2. Planarization of a microgear structure using CMP. An optical photograph is shown in Fig. 2a depicting the gear and the line profile step height measurement location. The pre- and post-polish step heights are shown in Fig. 2b. The small < 0.2 μm topography height variation remaining over the microgear is acceptable for micro-mechanical applications.

3. EVALUATION OF MICROMIRROR FLATNESS

A portion of the process flow used to demonstrate the initial micromirror structures is shown in Fig. 3. This section of the process (poly 2 definition through poly 3 mirror) includes the CMP planarization step. Not shown here are poly levels 0 and 1 which form additional wiring, flexures and support plates, pin joints and hinges, etc. Beginning with the polysilicon 2 layer, a 5.5 μm layer of SiO_2 is deposited using chemical vapor deposition. The oxide layer is subsequently planarized using CMP to a final thickness of 1.5 – 2.0 μm. Following CMP, we pattern the oxide and etch down to the underlying poly 2 layer, forming a "dimple cut". After the dimple cut, a 0.5 μm layer of SiO_2 is deposited. The wafers are then annealed at 1100 C for 3 hr to ensure a good, mechanically stable, "stress-free" polysilicon layer 2. After the anneal, a 2 μm layer of poly (layer 3) is deposited, patterned and etched to form the micromirror layer. Since the polysilicon layer conforms to the topography of the oxide surface, the front mirror surface reflects underlying topography prior to deposition.

Figure 4 shows a line scan profile of oxide material (using a Tencor P-11 system) after: (1) the CMP planarization step and (2) after the poly 2 layer anneal step. The oxide profile measurement is taken over 3 large hinge and support structures located at the poly 2 level as shown in the photograph (Fig. 4a). It is clear from the profile measurements shown in Fig. 4b that the topography actually worsens downstream from the CMP step due to the anneal process. During the anneal, the CVD SiO_2 material densifies and conforms to the underlying polysilicon structure. This increase in topography from approximately 30 nm following the CMP planarization to > 100 nm is unacceptable for adaptive optics micromirror applications.

4. REVISED PROCESS FLOW TO IMPROVE PLANARITY

After determining the root cause for the increase in topography, we investigated two variations to the baseline process: (1) perform an oxide CMP step after the high temperature anneal, and (2) maintain the baseline process flow up to the poly 3 level and planarize the poly 3 level using a poly CMP process. The latter process alternative provides an added benefit of

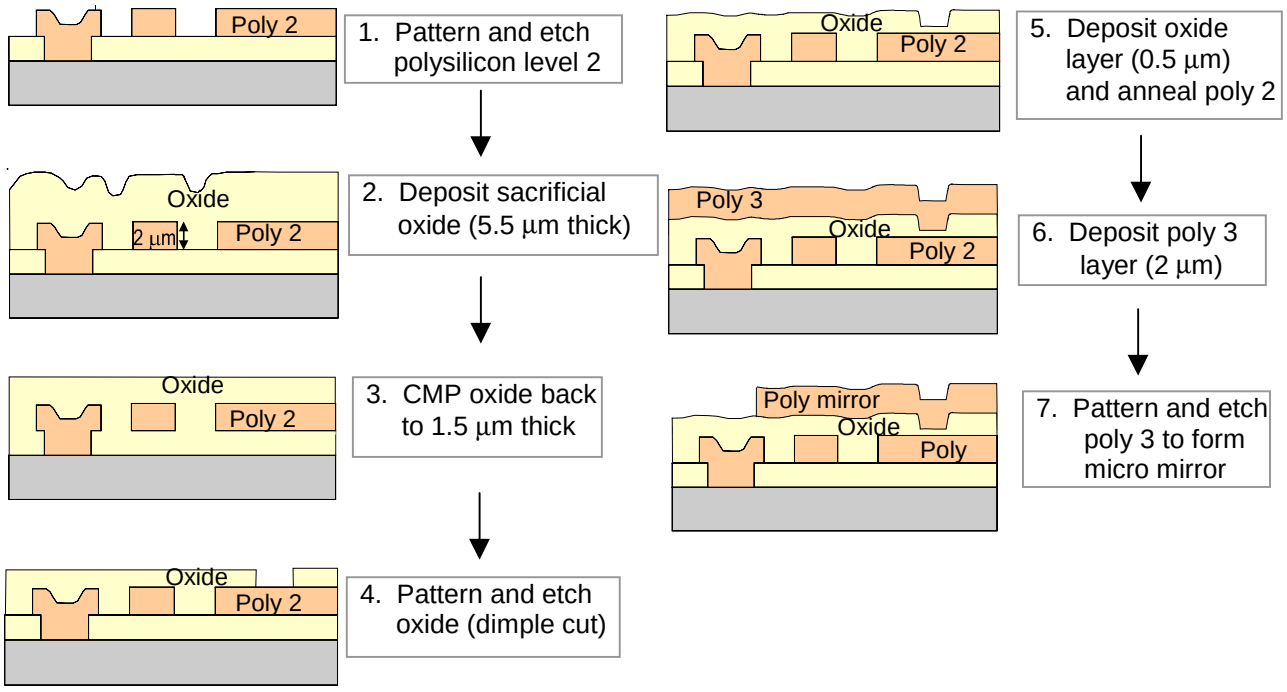
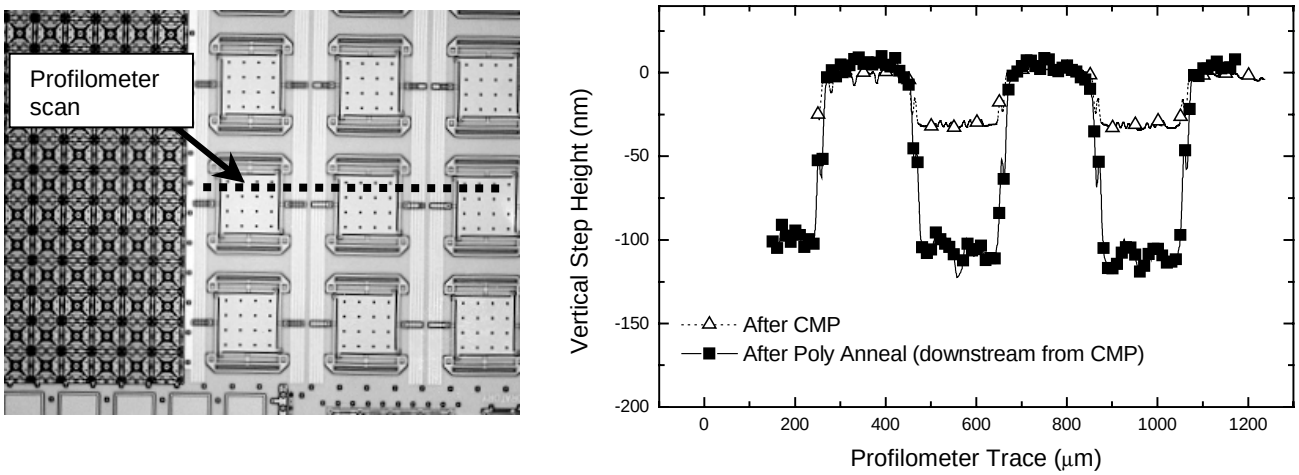


Figure 3. A portion of the process flow showing the fabrication steps from poly 2 level to poly3. The high temperature anneal step is performed after the CMP planarization step.

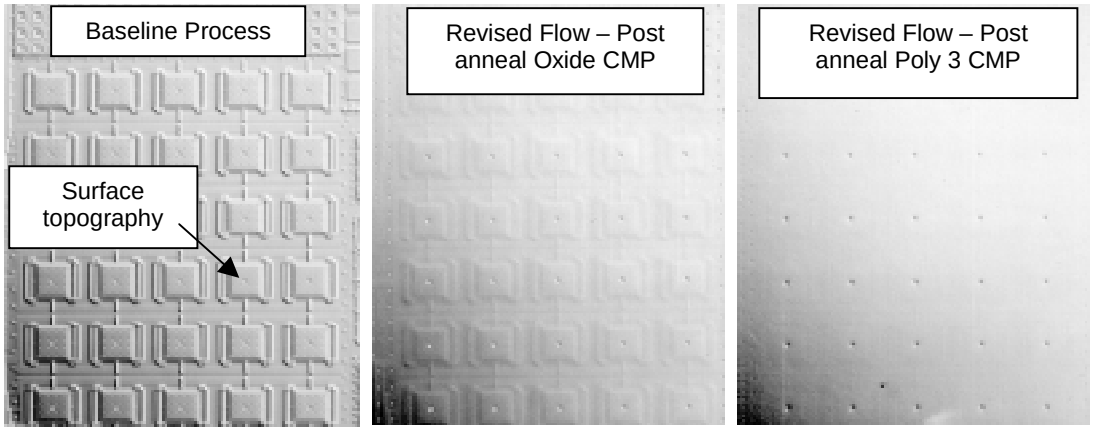


(a) (b)

Figure 4. Profilometer measurement of oxide material that lies above the mirror support features as shown in Fig. 4a.

providing a smooth as well as flat polysilicon surface, which should improve the overall micromirror performance [14]. Figure 5 shows three Nomarski mode optical microscope photographs imaged after deposition of the poly 3 layer for: (a) the baseline process, (b) modified oxide CMP step after the poly 2 anneal, and (3) modified process using baseline process up to poly 3 followed by a poly CMP planarization step. As shown in Fig. 5, the baseline process produces a high degree of contrast and clearly shows the effect of the underlying pattern which has printed through to the front mirror surface resulting in increased topography. As mentioned earlier, this result is unacceptable for micromirror applications. The second and third photographs correspond to the revised process flows described above. The Nomarski mode photographs given in Fig. 5b and

Fig. 5c show very significant topography reduction when compared to the baseline surface illustrated in Fig. 5a. Profilometer measurements for each of the process alternatives are given in Fig. 6 along with the baseline process as a reference. Both process alternatives (oxide CMP after the anneal or poly 3 CMP) provide acceptable < $\lambda/10$ wavelength flatness. The profilometer measurement that indicates the best result are with the second poly CMP process alternative (Δ step $_{max}$ = 20 nm). However, the effect of stress redistribution in the poly 3 layer due to an added CMP step has not been studied here and is currently under investigation.



(a) (b) (c)

Figure 5. Nomarski mode microscope photographs of the polysilicon 3 layer for (a) baseline process, (b) oxide CMP after the anneal step, and (c) baseline process with additional poly CMP step on poly 3 layer. The photographs give a good indication of the existing surface topography when viewed in the reflected light Nomarski interference contrast mode.

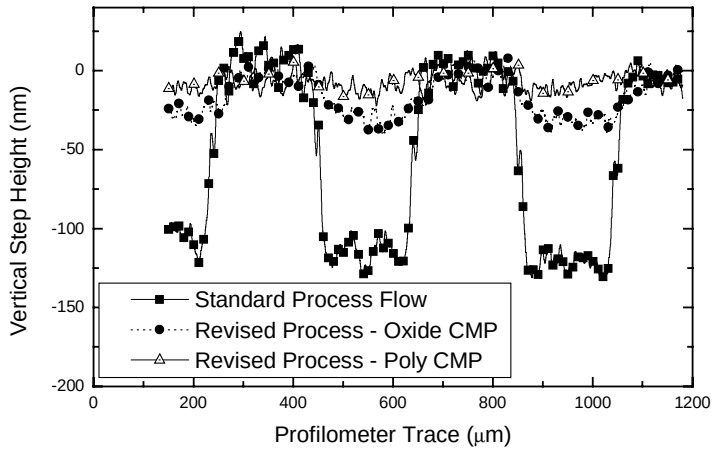


Figure 6. Profilometer measurement for the standard and revised process flows shown. Both of the revised process flows show an improvement in planarity and produce acceptable flatness for optical micromirror applications. The location of the profilometer scan is given in Fig. 4a.

5. SUMMARY AND CONCLUSIONS

In summary, we have discussed the planarization aspects for fabricating micromirror devices using chemical-mechanical polishing. Consideration must be given to the design layout, incoming film type to be planarized and associated step heights, and any downstream processes from CMP that may affect the overall planarity.

We have shown that a simple modification to an existing 4 level polysilicon surface micromachine process flow produces ultra-flat (< λ /10) polysilicon micromirror surfaces. The original topography generated in the baseline process was due to a high temperature anneal step, downstream from the sacrificial oxide CMP process step. This baseline process produced step heights ~ 100 nm, which was unacceptable for micro-optical device applications. Two solutions were presented: (1) perform an oxide CMP step following the high temperature anneal, and (2) perform a polysilicon CMP step after the poly 3 layer has been deposited. An added benefit to the latter option is that a smoother mirror surface is produced, which can result in improved mirror performance. Both process flow modifications demonstrated polysilicon surface flatness which meets requirements for micromirror applications.

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