3D Integration Technology for Highly Secure, Mixed Signal, Reconfigurable Systems

LDRD
LABORATORY DIRECTED RESEARCH & DEVELOPMENT

Sandia National Laboratories

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Problem

The NW community is challenged with developing system solutions that operate in harsh environments with a growing number of constraints such as:

- Fit significantly increased functionality into a fixed volume, reducing space for electronic subsystems and components
- Increased functionality must operate within fixed or reduced power budgets.
- Increasing security requirements
- Mixed mode ASICs are complex and non-optimized for either their digital or analog capabilities.
- Growing pin counts for ASICs to accommodate new system functionality and component redundancy requirements

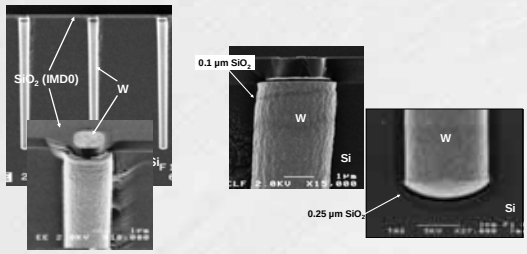
Approach

Enable a 3D chip stacking capability to reduce volume and power needs of electronic components while simultaneously improving security and responsiveness through reconfigurability. This work requires the following:

- Low-temperature processing that enables integration of dissimilar technologies
- Development of via formation and dielectric via isolation technology in the front-end of the Fab., which is compatible with post device fabrication temperature budget (<500 ˚C)
- Very smooth & flat surfaces with activation & also metal pads with different compositions for lower temperature (close to 100 ˚ C) wafer to wafer (W2W) and die to die (D2D) bonding
- Using metal combinations available in the Fab to develop low-temperature metal-to-metal bonding schemes
- Establishing high-fidelity modeling framework for 3D integrated electronics
- Development of methodology to create customized 3D architectures for different applications (viz. hybrid microsystems, anti-tamper systems, trusted computing, high performance computing, high pixel density sensor arrays)
- Multi-layer interconnect technologies that mitigate potential security vulnerabilities
- Architecture that provides hardware-based reconfigurability important for introducing novel surety solutions

Results

Fully FEOL-Compatible TSV Process with W Interconnect Material and Dielectric Isolation



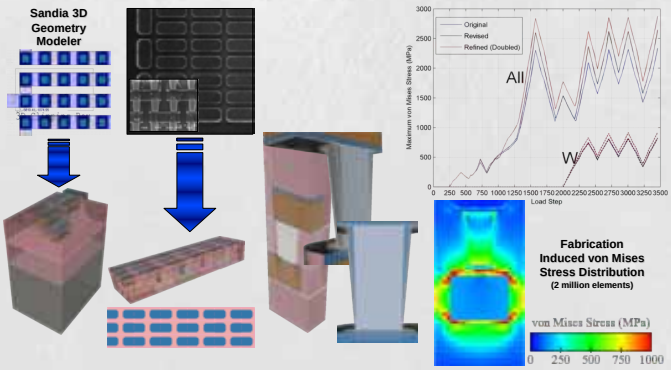
Low-Temperature Wafer to Wafer Bonding

SiO_2 to SiO_2 , 4 hr @ 100 ˚C

Al_2O_3 to Si, Room Temp. with anneal at 100 ˚C, 4Hr

Si Wafers with Patterned Test Structures

High-Fidelity Modeling to Assess Effect of Design Features on Process-Induced Stress



Significance

3D integration (3DI) enables the weapon system and subsystem design organizations to address the growing number of constraints for new systems by:

- Reducing volume and power required for electronic subsystems
- Improving security characteristics
- Leveraging optimized independently developed ASICs
- Enabling multiply redundant electronic subsystems to meet security and/or reliability requirements
- Reducing ASIC pin counts to simplify production issues

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