Engineering Few-electron-occupation Si Double Quantum Dots for Quantum Bits and Future Quantum Circuitry

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Problem

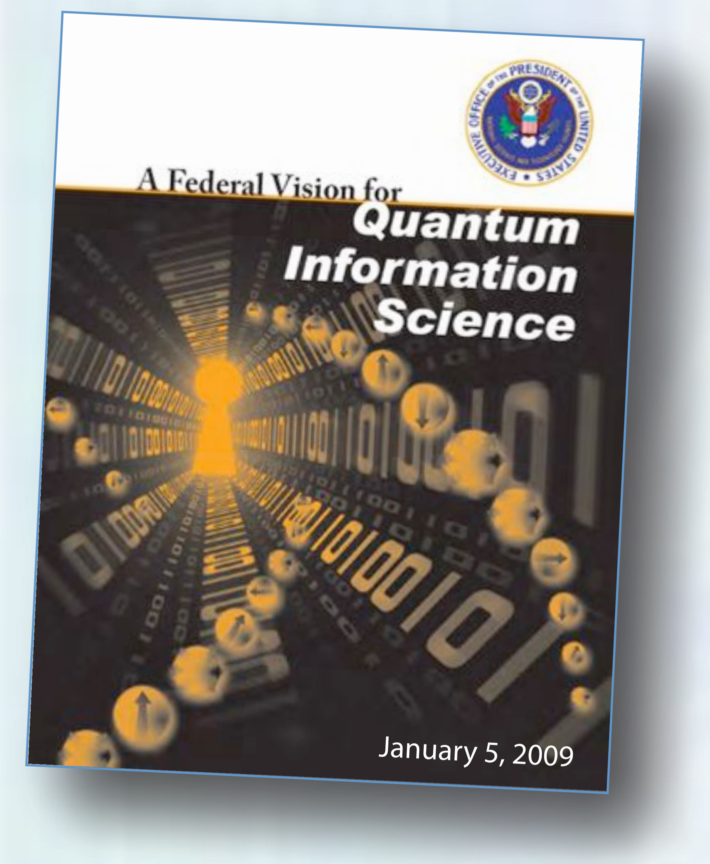
Quantum Information Science and Technology has National Importance

"**Quantum information science** …. creates a new conceptual platform for a family of **potentially disruptive technologies,** adding a new stage to the already staggering impact of conventional information technology."

"The ability to solve some of the "impossible" problems would enhance discovery and economic strength."

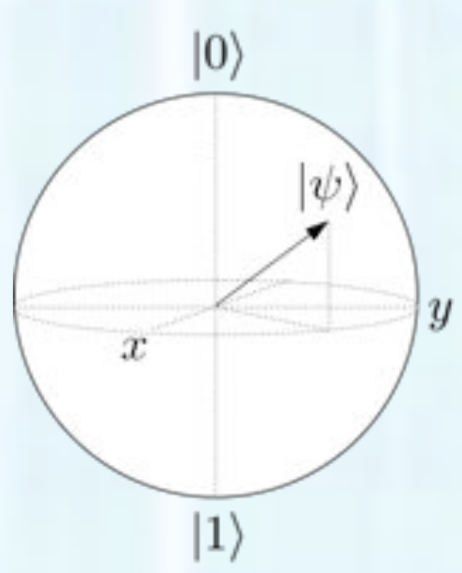
"…**applications** that rely on the "impossibility" of certain problems – widespread in data protection – would be rendered obsolete."

"**The United States' large stake** in all these potential applications **warrants a cohesive national effort** to achieve and maintain leadership in the rapidly emerging field of quantum information science."



Approach

Qubits and Single Qubit Gates



Transformation on qubits: Logic Gates

Bit

In	Out
0	0
1	1

In	Out
0	1
1	0

Qubit

NOT
$|0\rangle \to |1\rangle$
$|1\rangle \to |0\rangle$

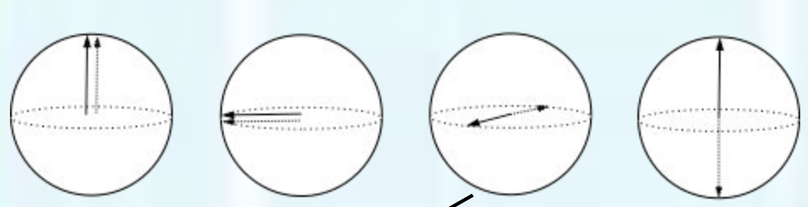
H
$|0\rangle \to (|0\rangle + |1\rangle)/\sqrt{2}$
$|1\rangle \to (|1\rangle - |0\rangle)/\sqrt{2}$

- A quantum bit can be any system that has two energy levels
- The QC information is described with a | 0 > and | 1 > basis
- A Bloch sphere is used to help picture the possible qubit states
- Single qubit gates produce superposition of the eigenstates who have non-zero probability amplitudes in each eigenstate

Spin Decoherence

90° X Rotation

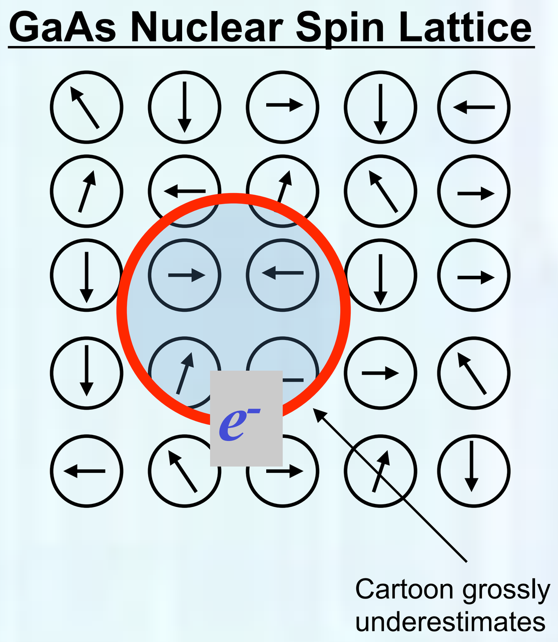
90° Rotation



Dashed spin evolves slower due to different field

Spin up/down result "randomized" due to inhomogeneous field

GaAs Nuclear Spin Lattice



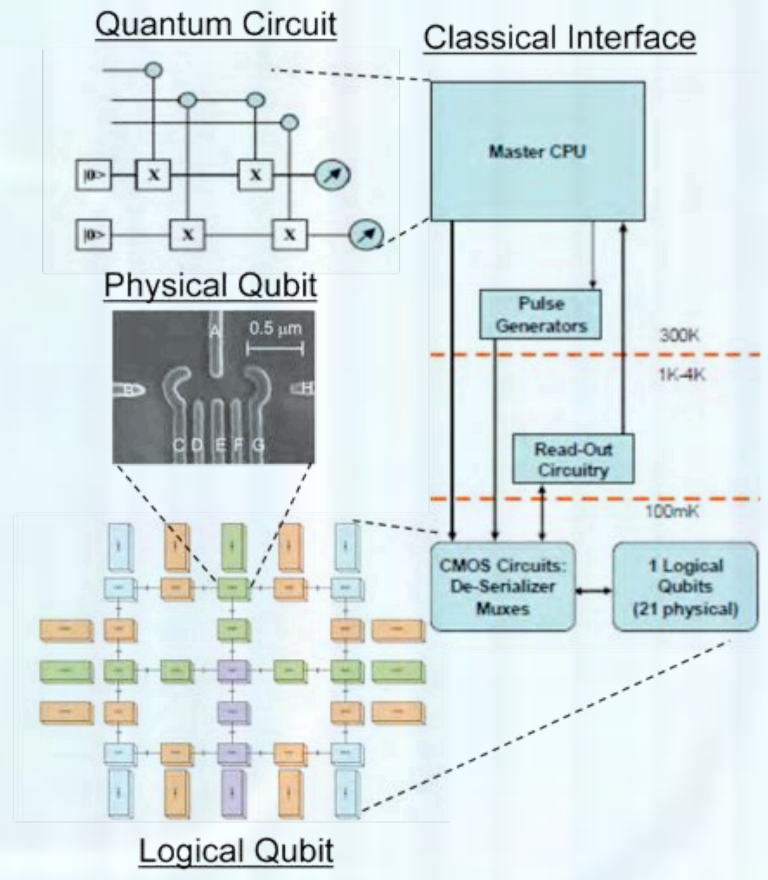
Cartoon grossly underestimates number of sampled nuclear spins

- Decoherence caused by non-ideal experimental conditions
- GaAs has demonstrated DQD Qubit but has an uncontrolled nuclear spin background (T_2 ~ 1- 10 μs)
- Long ensemble spin T_2 have been reported in silicon (~60 ms)
  - Reduced nuclear spin background when ^{29}Si reduced

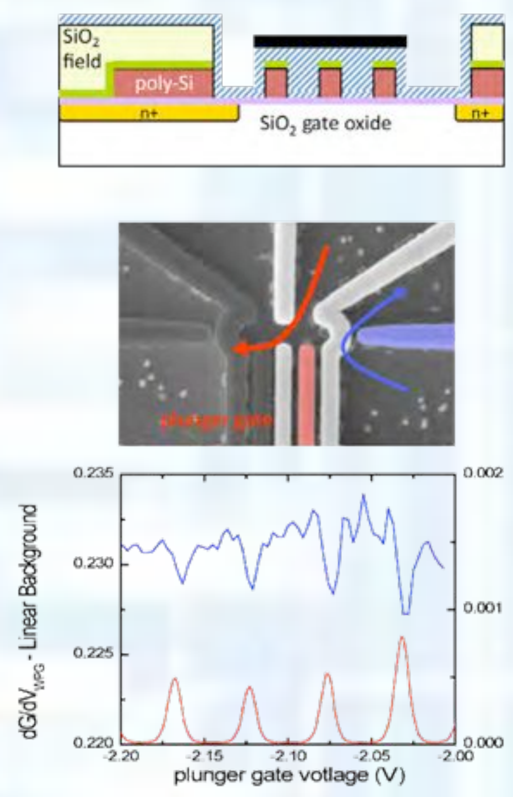
Results

Goals and Multidisciplinary Nature

- Create a double quantum dot qubit using Si MOS fabrication
  - Long T2 possible
- Design a quantum circuit to perform error correction
- Focus Areas
  - Physical Qubit
  - Electronics
  - Error Correction
  - Modeling
  - Second Generation Qubit



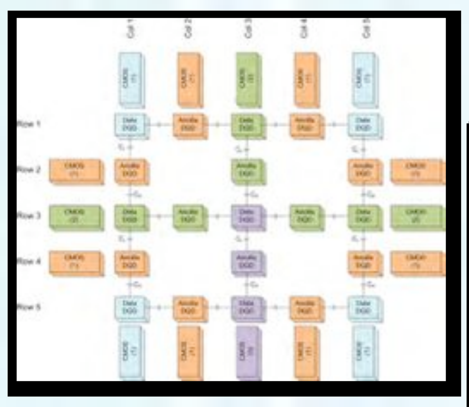
Single Electron Quantum Dots



- Quantum dots and tunnel barriers formed that do not exhibit disorder over large bias ranges
- Charge sensing is necessary for unambiguous identification of N=1 & future qubit gates
  - Charge sensing also potential improvement on measurement bottleneck
  - RF-electrometry & cryo circuit assisted approaches
  - Present sensitivity does not allow for fast sensing

Error Correction and Dynamic Decoupling

- Logical qubit
  - Combine multiple DQDs in an error-corrected architecture
- Sources of noise
  - Charge fluctuations
  - Spin noise
- Evaluate overall accuracy for different implementations
- Augment with dynamical decoupling to suppress idle error



$T = Z_{\pi/4}$	$\tau/2$	$p/2$
$\|1\rangle$	τ	$p/30$
M_Z	τ	$p/30$
$S = Z_{\pi/2}$	τ	p
$Z = Z_\pi$	2τ	$2p$
$X_{\pi/2}$	3τ	$4p$
$X = X_\pi$	4τ	$4p$
$CPHASE$	4τ	$4p$

Significance

Grand Challenge Summary

- *GC Vision:*
  - ***Develop silicon qubit hardware and develop the capability to assess the scalability to a logical qubit built with the hardware***
- **DQD qubit**
  - DQD fab characterization (mobility, valley splitting, Qf, Dit, …)
  - DQD: low disorder QD
  - *DQD: charge sensing in lateral MOS QD [world first in || w/ UCLA]*
  - Extra ^{3}He system being installed (in progress)
- **2nd Generation DQD structures**
  - SiGe successfully grown on sSOI
  - Few donor devices nearly completed
  - SIGMA proof of principle (100%DE, P_{dark}~10^{-4})

Beat disorder make N~1 QD

- **Quantum-classical interface**
  - 4K CMOS models completed & now being refined (V_t, S, I_d, etc.)
  - 4K circuits tested & following-up on *external requests*
  - Electronics constraints for BS9 (21) memory (30 ns gate)

Enabling tech & Constraints

- **Logical qubit design**
  - Initial p_c of logical qubit w/hardware constraints (p_c~ 10^{-4})
  - Transport and gate guidance
  - Dynamic decoupling guidance => estimated T_2^* impact

Guidance on what we need

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND2009-4901P

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